Quad, High Voltage, Amplifier Array

Features

- Four independent high voltage amplifiers
- 190V output swing
- 9.0V/µs typical output slew rate
- Fixed gain of 66.7V/V
- High value internal feedback resistors
- Very low operating current

Applications

- Tunable Laser
- MEMS driver
- Test equipment
- Piezoelectric transducer driver
- Braille driver

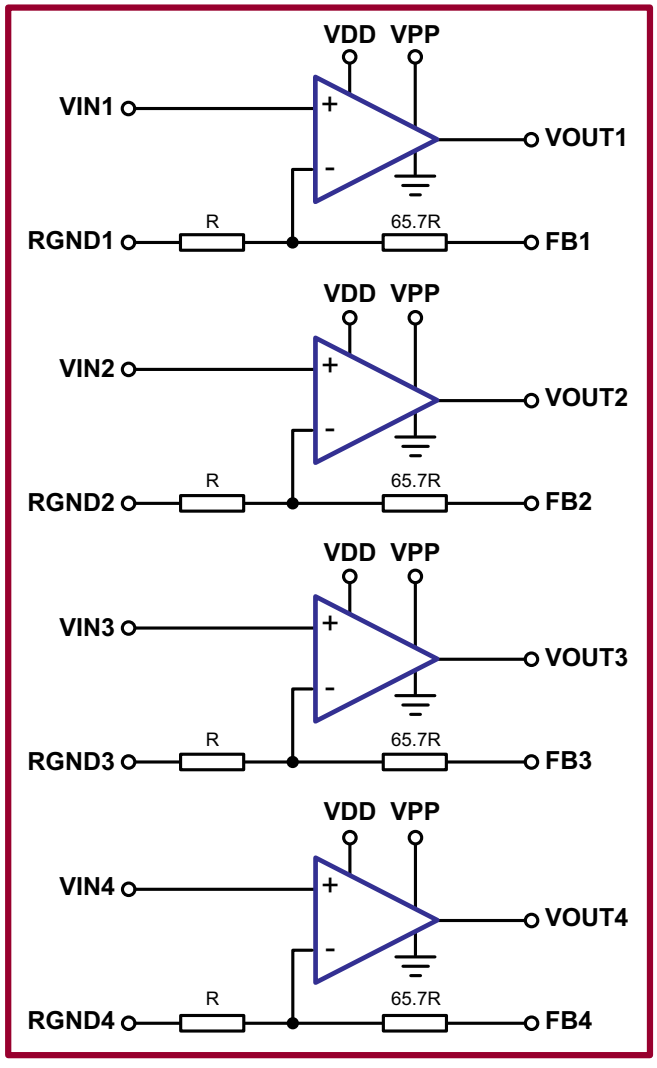
General Description

The Supertex HV264 is a quad high voltage amplifier array integrated circuit. It operates on a 200V high voltage supply and a 5.0V low voltage supply. Each channel has its own input and output.

When both VOUT and FB pins are connected together and RGND is set at 0V, a non-inverting amplifier is formed with closed loop gain of 66.7V/V. High value internal feedback resistors are used to minimize the power dissipation. The input voltage V_{IN} is designed for a range of 0.05V to 2.85V. The output can swing from 1.0V to V_{PP} -10V. A 2.85V input will cause the output to swing to 190V.

The HV264 is designed for maximum performance with minimal high voltage current. The high voltage current for each channel is less than 75µA. The typical output slew rate performance is 9.0V/µs.

Block Diagram



Ordering Information

Part Number	Package Option	Packing
HV264TS-G	24-Lead TSSOP	2500/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

ESD Sensitive Device

Absolute Maximum Ratings

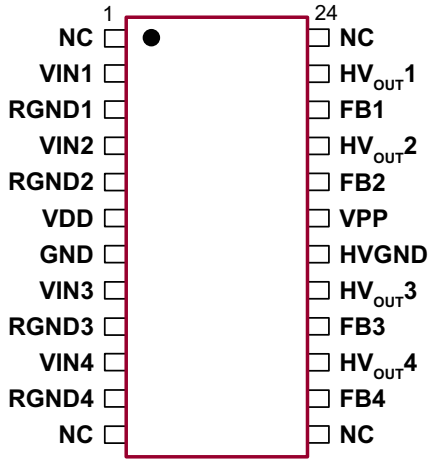
Parameter	Value
V_{PP}, High voltage supply	225V
V_{DD}, Low voltage supply	6.5V
HV_{OUT}, Output voltage	0V to VPP
V_{IN}, Analog input signal	0V to VDD
Storage temperature range	-65°C to 150°C
Maximum junction temperature	150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Resistance

Package	θ_{ja}
24-Lead TSSOP	72°C/W

Pin Configuration

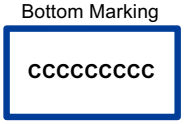


24-Lead TSSOP
(top view)

Product Marking

Top Marking

Bottom Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID
_____ = "Green" Packaging
**May be part of ejector pin*

Package may or may not include the following marks: Si or

24-Lead TSSOP

Operating Conditions

Sym	Parameter	Min	Typ	Max	Unit	Conditions
V_{PP}	High voltage positive supply	50	-	200	V	---
V_{DD}	Low voltage positive supply	4.5	5.0	5.5	V	---
R_{GND}	Input ground range	0	0	V_{DD}	V	---
I_{PP}	V_{PP} supply current	-	-	300	µA	V_{PP} = 200V, All inputs at 0V
I_{DD}	V_{DD} supply current	-	-	5.0	mA	V_{DD} = 5.5V
T_A	Ambient temperature range	-40	-	85	°C	---
T_J	Junction temperature range	-40	-	100	°C	---

Power Up / Down Sequence

The device can be damaged due to improper power up / down sequence. To prevent damage, please follow the acceptable power up / down sequences and add an external diode across VPP and VDD, where the anode of the diode is connected to VDD and the cathode is connected to VPP. Any low current high voltage diode such as a 1N4004 will be adequate.

Acceptable Power Up Sequences

1) V_{DD} 2) V_{PP} 3) Inputs
1) V_{DD} 2) Inputs 3) V_{PP}

Acceptable Power Down Sequences

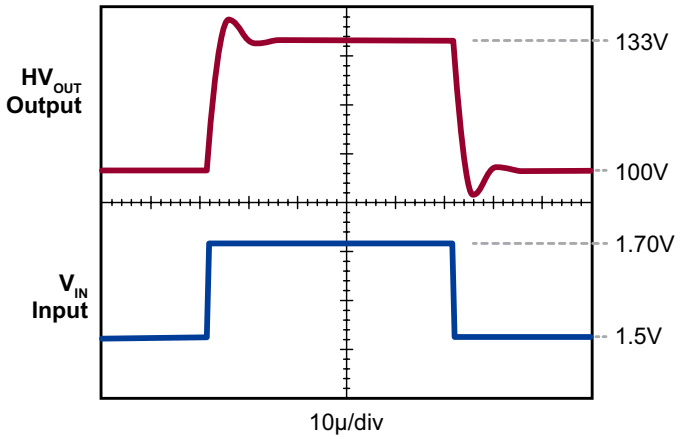
1) Inputs 2) V_{PP} 3) V_{DD}
1) V_{PP} 2) Inputs 3) V_{DD}

Electrical Characteristics

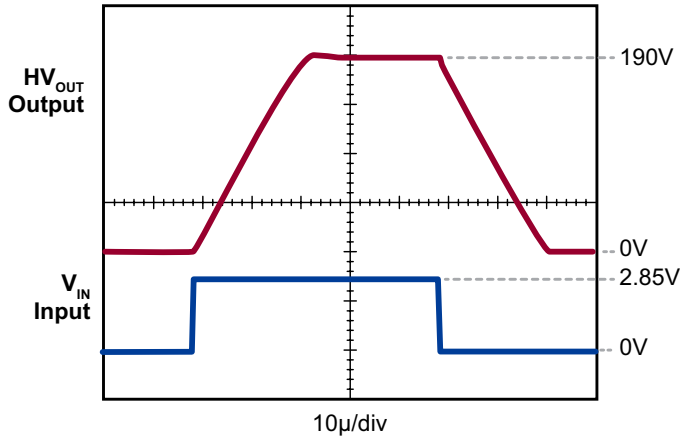
(Over operating conditions unless otherwise noted, T_J = 25°C.)

Sym	Parameter	Min	Typ	Max	Unit	Conditions
High Voltage Amplifier Output						
HV_{OUT}	HV_{OUT} voltage swing	1.0	-	V_{PP} -10	V	No Load
I_{SINK}	HV_{OUT} sink current	3.0	-	-	mA	---
I_{SOURCE}	HV_{OUT} source current	3.0	-	-	mA	---
V_{IN}	Input voltage range	0	-	V_{DD} -1.5	V	---
I_{IN}	V_{IN} input current	-	-	50	nA	---
HV_{OS}	HV_{OUT} DC offset	-	-	±1.0	V	V_{IN} = 0.2V
SR	HV_{OUT} slew rate - rising edge	5.0	9.0	30	V/µs	V_{PP} = 200V, Load = 15pF, measured between 10% to 90% of HV_{OUT}
	HV_{OUT} slew rate - falling edge	-	9.0	-		
R_{FB}	Feedback impedance, $R_f + R_i$	3.5	5.3	-	MΩ	---
A_V	Closed loop gain	63.4	66.7	70.0	V/V	---
BW	HV_{OUT} -3dB channel bandwidth	25	-	-	kHz	V_{PP} = 200V, Load = 15pF
C_{LOAD}	HV_{OUT} capacitive load	0	-	15	pF	---
V_N	Output referred noise	-	-	10	mV_{RMS}	Measured at HV_{OUT}, 0 to 1.0kHz single-pole, V_{IN} = 0.2V
PSRR	V_{DD} power supply rejection ratio	55	-	-	dB	V_{DD} = 4.5 to 5.5V V_{PP} = 200V, V_{IN} = 0.1V
PSRR	V_{PP} power supply rejection ratio	60	-	-	dB	V_{DD} = 5.0V V_{PP} = 50 to 200V, V_{IN} = 0.1V
Xtalk	Crosstalk	-	-	-80	dB	Output referred

Typical Small Signal Pulse Response

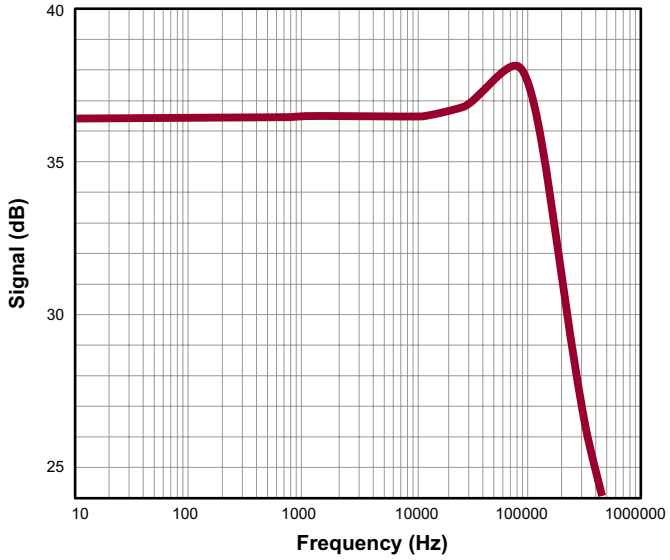


Typical Large Signal Pulse Response



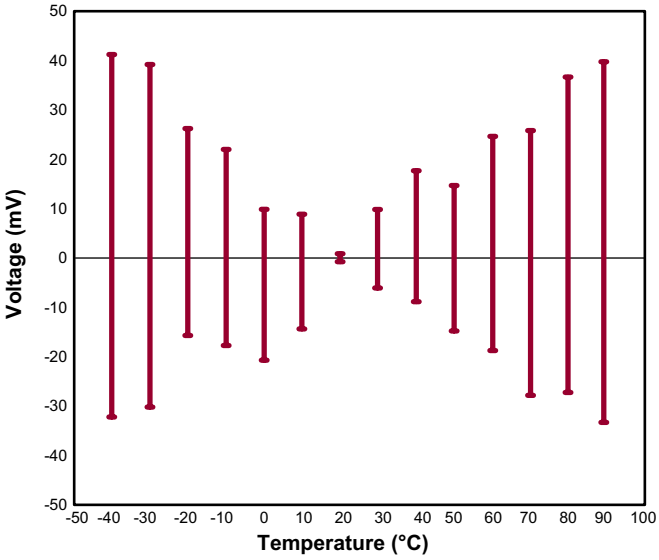
Typical Bode Plot of Small Signal Gain

(V_{IN} = 0.2V_{P-P}, V_{DC} = 1.5V, V_{DD} = 5.0V, V_{PP} = 200V)



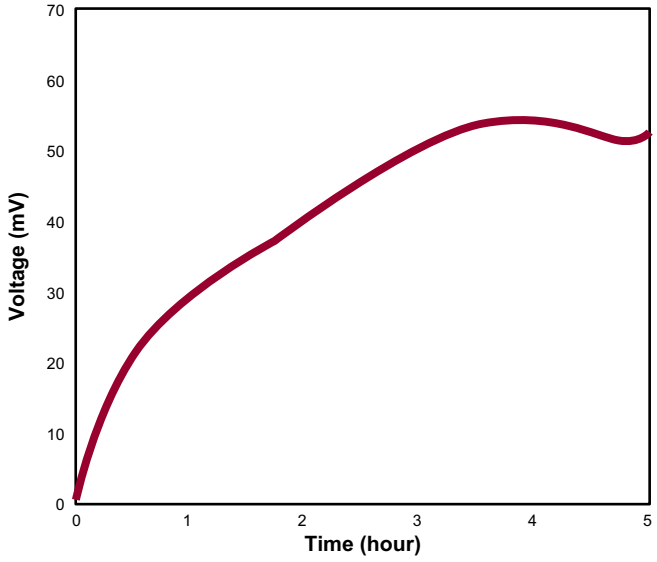
Distribution of Typical HVOUT Deviation Over Temperature

(V_{IN} = 0.1VDC, 1.6VDC, 3.3VDC, in reference to 20°C)



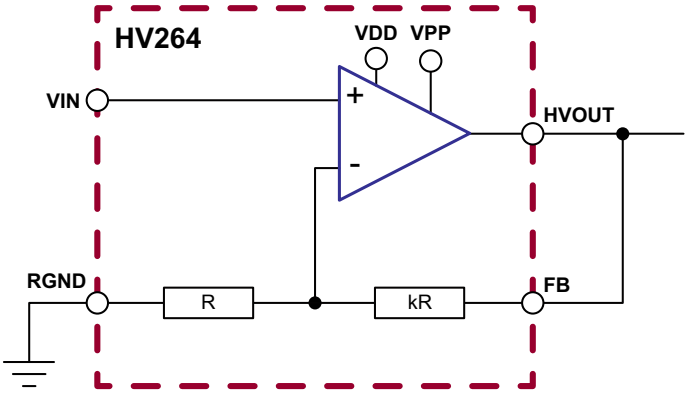
Typical HVOUT Drift Over Time

(V_{PP} = 200V, V_{DD} = 5.5V, $_{VIN}$ = 0.2V, Room Temperature, 50pF Output Loading)

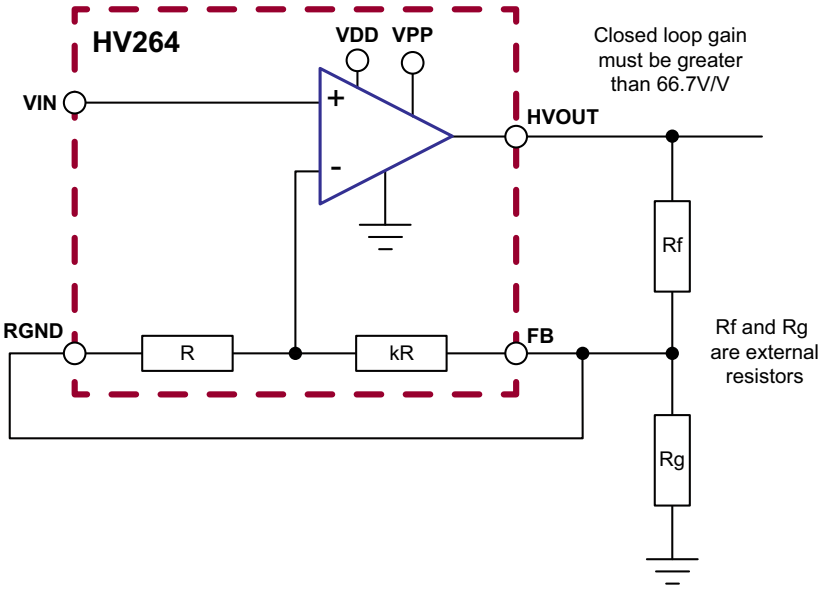


Typical Application Circuits

With Internal Gain Setting Resistors



With External Gain Setting Resistors

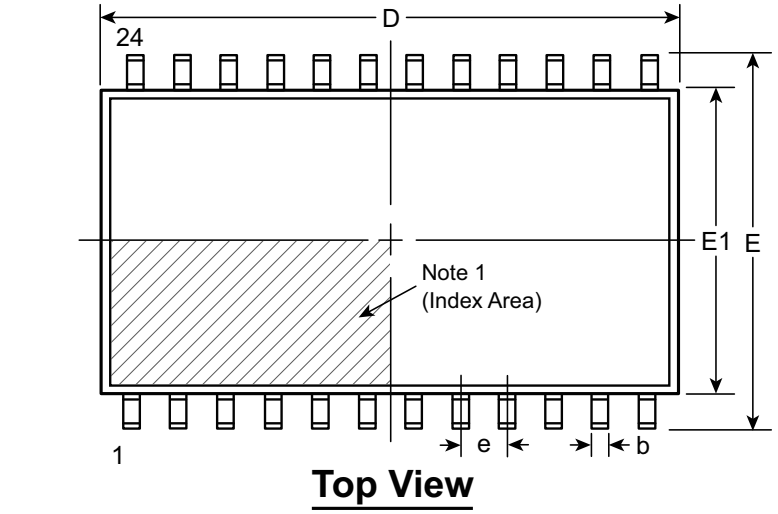


Pin Description - 24-Lead TSSOP

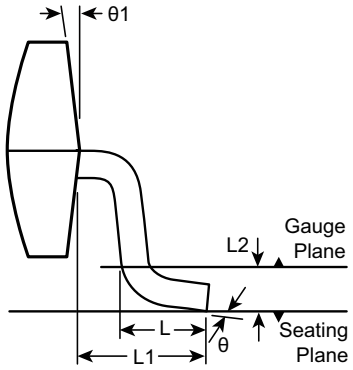
Pin	Name	Description
1	NC	No Connection
2	VIN1	Amplifier input 1
3	RGND1	Resistor ground for channel 1. Typically grounded. Can be connected to a voltage source to create a DC offset.
4	VIN2	Amplifier input 2
5	RGND2	Resistor ground for channel 2. Typically grounded. Can be connected to a voltage source to create a DC offset.
6	VDD	Low voltage positive supply
7	GND	Device ground
8	VIN3	Amplifier input 3
9	RGND3	Resistor ground for channel 3. Typically grounded. Can be connected to a voltage source to create a DC offset.
10	VIN4	Amplifier input 4
11	RGND4	Resistor ground for channel 4. Typically grounded. Can be connected to a voltage source to create a DC offset.
12	NC	No Connection
13	NC	No Connection
14	FB4	Feedback input 4
15	HVOUT4	Amplifier output 4
16	FB3	Feedback input 3
17	HVOUT3	Amplifier output 3
18	HVGND	Device high voltage supply ground
19	VPP	High voltage positive supply
20	FB2	Feedback input 2
21	HVOUT2	Amplifier output 2
22	FB1	Feedback input 1
23	HVOUT1	Amplifier output 1
24	NC	No Connection

24-Lead TSSOP Package Outline (TS)

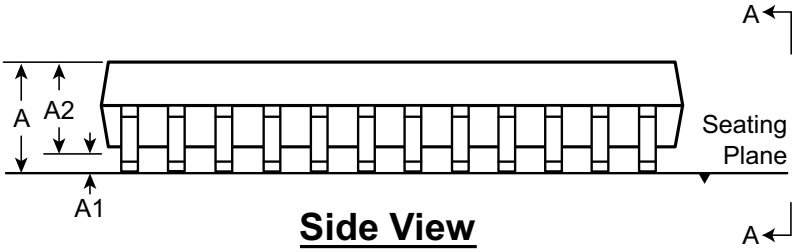
7.80x4.40mm body, 1.20mm height (max), 0.65mm pitch



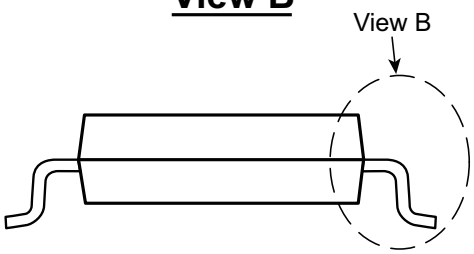
Top View



View B



Side View



View A-A

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	0.85*	0.05	0.80	0.19	7.70	6.20*	4.30	0.65 BSC	0.45	1.00 REF	0.25 BSC	0°	12° REF
	NOM	-	-	1.00	-	7.80	6.40	4.40		0.60			-	
	MAX	1.20	0.15	1.15†	0.30	7.90	6.60*	4.50		0.75			8°	

JEDEC Registration MS-153, Variation AD, Issue F, May 2001.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings are not to scale.
***Supertex** Doc. #: DSPD-24TSSOPTS, Version B041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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