ANALOG DEVICES

EVAL-AD7293SDZ User Guide
UG-817

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluating the AD7293 12-Bit Power Amplifier Current Controller with ADC, DACs, Temperature and Current Sensors

FEATURES

Full featured evaluation board for AD7293
Graphical user interface (GUI) software with USB control
Various link options

EVALUATION KIT CONTENTS

AD7293 evaluation board
AD7293 evaluation board software CD

EQUIPMENT NEEDED

EVAL-SDP-CB1Z
Bench top power supply and connector cables

APPLICATIONS

GaN and GaAs power amplifier (PA) monitoring and controls
Base station power amplifiers
General-purpose system monitoring and controls

ONLINE RESOURCES

Documents Needed
- **AD7293 data sheet**
- **AD7293 evaluation board software**

Design and Integration Files
- **Schematics, layout files, bill of materials**

GENERAL DESCRIPTION

This user guide describes the evaluation board for the AD7293, which is a 12-bit monitoring device with a multichannel ADC, DACs, and temperature and current sensors.

For full details on the AD7293, see the AD7293 data sheet and consult it when using the EVAL-AD7293SDZ. The configuration of the various link options is explained in the Evaluation Board Hardware section.

The EVAL-AD7293SDZ requires the EVAL-SDP-CB1Z board. The EVAL-AD7293SDZ interfaces to the USB port of the PC via the EVAL-SDP-CB1Z. Software that allows the user to easily program the AD7293 is available with the EVAL-AD7293SDZ.

EVAL-AD7293SDZ AND EVAL-SDP-CB1Z CONNECTION PHOTOGRAPH

Figure 1.

TABLE OF CONTENTS

REVISION HISTORY

7/2016—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

AD7293 POWER SUPPLY

There are several options available for powering the EVAL-AD7293SDZ, all of which use external power supplies.

The default option for powering the EVAL-AD7293SDZ is to supply J11 or J12 with 9 V.

Supply approximately 8 V to J2, LK_PAVDD (see the Closed-Loop Current Control section and Table 5) with a current limit to avoid a current path to ground via the BSS159 depletion mode transistor.

The supply planes are decoupled to the relevant ground plane using 10 µF and 0.1 µF ceramic capacitors connected to the EVAL-AD7293SDZ. The EVAL-AD7293SDZ requires a number of power supply inputs: AVDD, VDD, VDRIVE, AVSS, DACVDD-UNI, and DACVDD-BI.

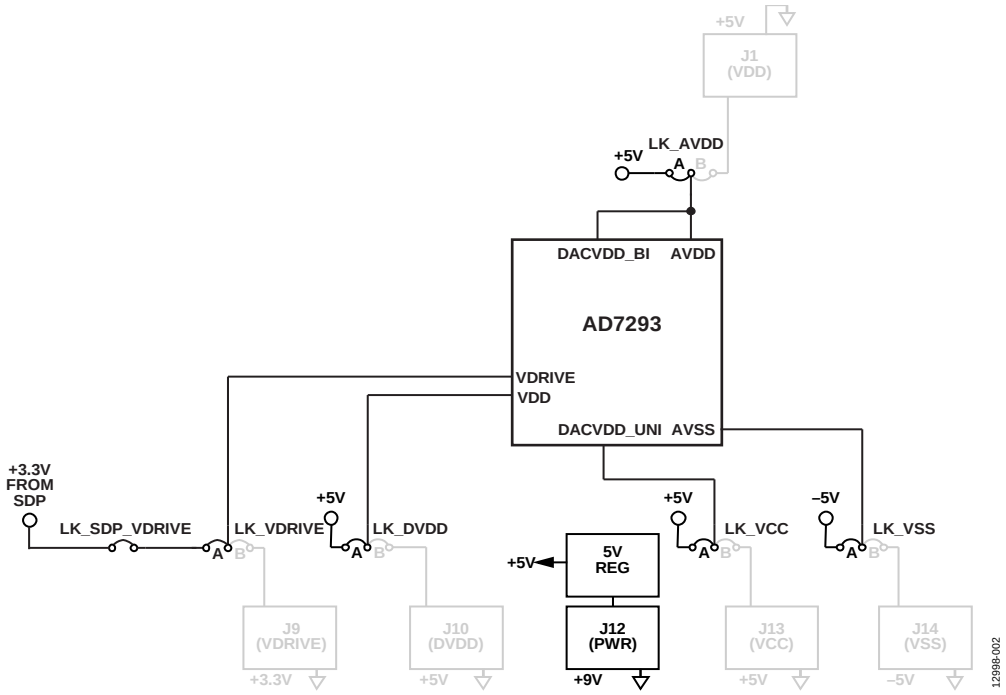


Figure 2. AD7293 Power Connector Defaults and Necessary Supply Voltages

Figure 3. EVAL-AD7293SDZ Power Connections

Table 1. Connector Functions

Connector	Description
J1-1	External analog VDD power connector
J1-2	GND power connector
J2-1	External PAVDD power connector
J2-2	GND power connector
J3-1	VPP0 power connector
J3-2	GND power connector
J4-1	VPP1 power connector
J4-2	GND power connector
J5-1	VPP2 power connector
J5-2	GND power connector
J6-1	VPP3 power connector
J6-2	GND power connector
J9-1	VDRIVE power connector
J9-2	GND power connector
J10-1	DVDD power connector
J10-2	GND power connector
J11-1	PWR (9 V) power connector
J11-2	GND power connector
J12	Alternative PWR (9 V) power connector
J13-1	AVCC unipolar DAC supply power connector
J13-2	GND power connector
J14-1	AVSS negative supply power connector
J14-2	GND power connector

Table 2. Power Supply Link Options

Link Mnemonic	Description
LK_AVDD	This link selects the analog VDD supply for the EVAL-AD7293SDZ. Position A: selects the 5 V regulated supply coming from the ADP7104 voltage regulator. Position B: selects the external VDD (J1) located at the top of the board (default).
LK_VDRIVE	This link selects the logic supply level for the AD7293. Position A: selects 3.3 V that is supplied from the EVAL-SDP-CB1Z (default). Position B: selects an external VDRIVE (J9) located at the bottom left corner of the board.
LK_VCC	This link selects the positive supply for the unipolar DACs. Position A: selects the 5 V regulated supply coming from the ADP7104 voltage regulator. Position B: selects the external AVCC (J13) located at the bottom of the board (default).
LK_VSS	This link selects the negative supply for the bipolar DACs. Position A: selects the −5 V regulated supply coming from the ADP3605 voltage regulator. Position B: selects the external AVSS (J14) located at the bottom of the board (default).
LK_DVDD	This link selects the supply for the AD7293 digital supply. Position A: selects the 5 V regulated supply coming from the ADP7104 voltage regulator. Position B: selects the external DVDD (J10) located at the bottom of the board (default).
LK_DVDD1	This link selects the supply for MC74HC244A. Position A: selects the DVDD (J10) as the supply for the MC74HC244A. Position B: selects GND as the supply for the MC74HC244A.
LK_PAVDD	This link selects the supply for the PAVDD node on the EVAL-AD7293SDZ. Position A: selects the 5 V regulated supply coming from the ADP7104 voltage regulator. Position B: selects the external PAVDD (J2) located at the top of the board.
5V_EXT	This external 5 V link connects J1 to the 5 V node.
5V_REG	This link (L9) connects the 5 V regulator output to the 5 V node.

SERIAL COMMUNICATION, GPIO, AND SYSTEM DEMONSTRATION PLATFORM (SDP)

The EVAL-SDP-CB1Z (SDP-B), system demonstration platform, handles communication to the EVAL-AD7293SDZ via the PC. The SDP-B may require power from the EVAL-AD7293SDZ depending on the current available from the PC USB interface it is connected to. The default option leaves LK_SDP_PWR disconnected, and the logic level is taken from the EVAL-SDP-CB1Z (3.3 V) by inserting LK_SDP_VDRIVE.

The default for the $\overline{\text{RESET}}$, GPI07/LDAC, and GPIOx/SLEEPx pins on the AD7293 is controlled by the hardware on the EVAL-AD7293SDZ. Use the GPI07/LDAC, SLEEP0, and SLEEP1 jumpers to tie the inputs high (not inserted) or low (inserted). Control $\overline{\text{RESET}}$ using the push-button interface (low when pushed).

Route the pins out to J8 via the options on the LK_RESET, LK_SLEEP0, LK_SLEEP1, and LK_LDAC links. See Figure 25 and Figure 26 for additional information.

Table 3. Serial Communication Link Options

Link Mnemonic	Description
LK_SDP_PWR	Insert to provide 5 V power to the EVAL-SDP-CB1Z.
LK_SDP_VDRIVE	Insert to take the 3.3 V digital signal high level from the SDP as the reference for the serial peripheral interface.
LK_SLEEP0	This link determines whether the GPIO5/SLEEP0 pin is controlled by the SDP or by the SLEEP0 link on the EVAL-AD7293SDZ. Position A: the pin is controlled by the SDP. Position B: the pin is controlled by the SLEEP0 link and pull-up on the EVAL-AD7293SDZ (default).
SLEEP0	If Link B is selected on LK_SLEEP0, this link controls the polarity of the GPIO5/SLEEP0 pin. If inserted, the signal is pulled low. If not inserted, the signal is pulled high.
LK_SLEEP1	This link determines whether the GPIO6/SLEEP1 pin is controlled by the SDP or by the SLEEP0 link on the EVAL-AD7293SDZ. Position A: the pin is controlled by the SDP. Position B: the pin is controlled by the SLEEP1 link and pull-up on the EVAL-AD7293SDZ (default).
SLEEP1	If Position B is selected on LK_SLEEP0, this link controls the polarity of the GPIO6/SLEEP1 pin. If inserted, the signal is pulled low. If not inserted, the signal is pulled high.
LK_RESET	In conjunction with LK_RESET/GPIO0, this link determines whether the $\overline{\text{RESET}}$ pin is controlled by the SDP or by the RESET link on the EVAL-AD7293SDZ. Position A: the pin is controlled by the SDP. Position B: the pin is controlled by the RESET push-button EVAL-AD7293SDZ (default).
LK_RESET/GPIO	This link determines whether the signal coming from the SDP controls the $\overline{\text{RESET}}$ pin via LK_RESET or the GPIO0 pin. Position A: The $\overline{\text{RESET}}$ pin is controlled by the SDP. Position B: The GPIO pin is controlled by the SDP.
LK_LDAC	This link determines whether the GPIO7/LDAC pin is controlled by the SDP or by the LDAC link on the EVAL-AD7293SDZ. Position A: the pin is controlled by the SDP. Position B: the pin is controlled by the LDAC link and pull-up on the EVAL-AD7293SDZ (default).
LDAC	If Position B is selected on LK_LDAC, this link controls the polarity of the GPIO7/LDAC pin. If inserted, the signal is pulled low. If not inserted, the signal is pulled high.

CLOSED-LOOP CURRENT CONTROL

The EVAL-AD7293SDZ has four independent closed-loop drain current controllers. By default, the control loops are populated on the EVAL-AD7293SDZ with all the necessary components, such as a sense resistor, and the closed-loop software window operates with a single loop (Loop 0).

LK_PAVDD supplies the voltage (8 V). This current flows through a PMOS switch controlled by the PA_ON pin.

The PMOS can be turned on and off by using the supplied evaluation software that allows the user to decide when current is supplied to the sense resistor high side.

LK_PMOS/RSO selects if PMOS circuitry is part of the loop.

The EVAL-AD7293SDZ contains a BSS159N depletion mode, low voltage transistor that mimics the characteristics of a higher power depletion mode PA but at lower voltages.

By default, the loops are connected to the BSS159N. R_0 and C_0 are populated with a resistor and a capacitor to form the filter with a time constant of 5 ms to 50 ms.

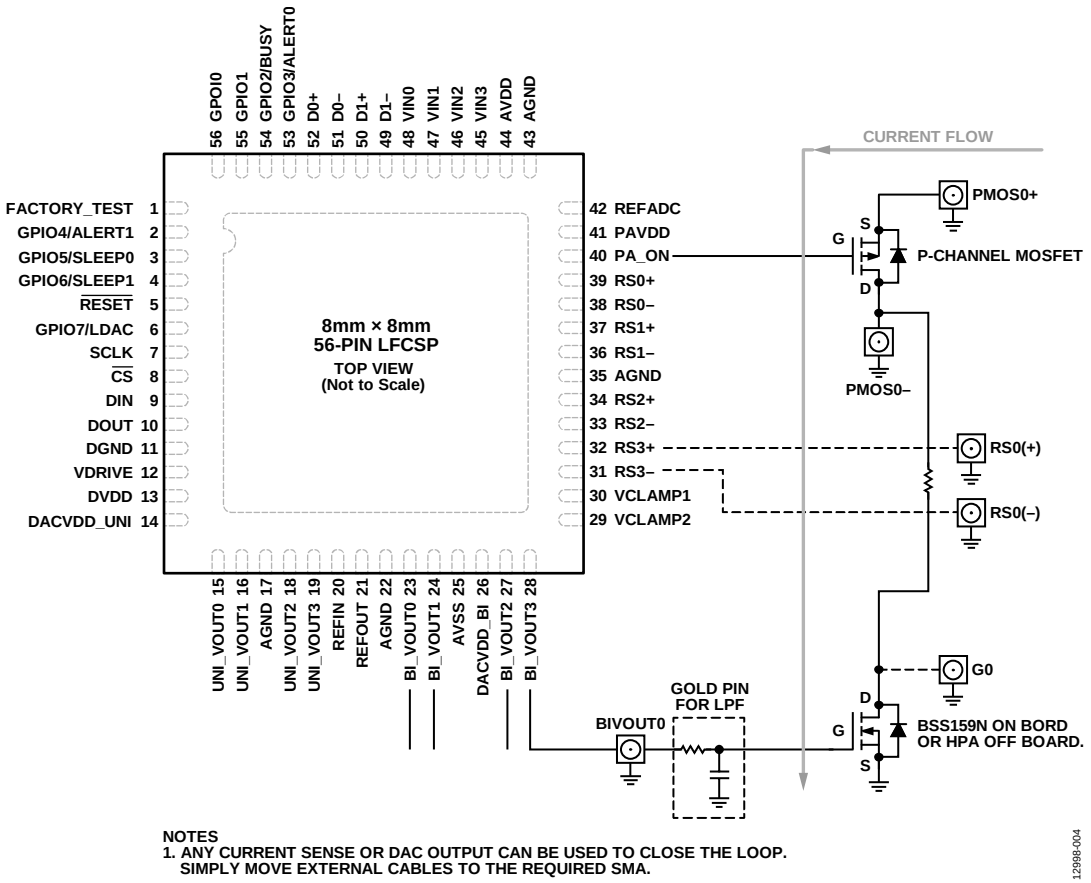


Figure 4. EVAL-AD7293SDZ Loop Configuration

Table 4. PA_ON Link Options

Link Mnemonic	Description
PMOS_S	This link selects the source/supply of the PMOS switch. Position A: selects PMOS1+, Loop 1 (for the supply to be connected, LK_PMOS/RS1 must be in Position A). Position B: selects PMOS0+, Loop 0 (for the supply to be connected, LK_PMOS/RS0 must be in Position B) (default).
LK_PMOS/RS3	This link selects the routing of the drain of the PMOS switch. Position A: selects the top of the high-side of the RS1(+) pin. Position B: selects the top of the high-side of the RS0(+) pin (default).

Table 5. Loop Power Supply Options

Link Mnemonic	Description
LK_PAVDD	This link selects the supply for the PAVDD node on the EVAL-AD7293SDZ. Position A: selects the 5 V regulated supply coming from the ADP7104 voltage regulator (default). Position B: selects the external PAVDD (J2) located at the top of the board.
LK_VPP0	This link selects the VPP0 supply for Loop 0 on the EVAL-AD7293SDZ. Position A: selects the 5 V regulated supply coming from the ADP7104 voltage regulator (default). Position B: selects the external VPP0 (J3) located at the top of the board. Position C: selects the PAVDD supply that is controlled by the LK_PAVDD.
LK_PMOS/RS0	This link selects whether the PA_ON controller is part of Loop 0 or the user can connect directly to the top of the sense resistor at the RS0(+) node. Position A: connects directly to the top of the RSENSE0 resistor at the RS0(+) node. Position B: PMOS0+ connects to the PA_ON control circuit (default).
LK_VPP1	This link selects the VPP1 supply for Loop 1 on the EVAL-AD7293SDZ. Position A: selects the 5 V regulated supply coming from the ADP7104 voltage regulator (default). Position B: selects the external AVPP1 (J4) located at the top of the board. Position C: selects the PAVDD supply that is controlled by the LK_PAVDD link.
LK_PMOS/RS1	This link selects whether the PA_ON controller is part of Loop 1 or the user can connect to the top of the sense resistor at the RS1(+) node. Position A: PMOS1+ connects to the PA_ON control circuit. Position B: connects directly to the top of the RSENSE1 resistor at the RS1(+) node (default).
LK_VPP2	This link selects the VPP supply for Loop 2 on the EVAL-AD7293SDZ. Position A: selects the 5 V regulated supply coming from the ADP7104 voltage regulator (default). Position B: selects the external VPP2 (J5) located at the top of the board.
LK_VPP3	This link selects the VPP supply for Loop 3 on the EVAL-AD7293SDZ. Position A: selects the 5 V regulated supply coming from the ADP7104 voltage regulator (default). Position B: selects the external VPP3 (J6) located at the top of the board.

Table 6. Closed-Loop (EVAL-AD7293SDZ Closed-Loop Board) Current Control Transistor Options

Link Mnemonic	Description
D_PA0	This link selects the drain connector to the BSS159N. Inserted: selects the bottom of the RS0(−) sense resistor. Not inserted: BSS159N drain not connected to Loop 0.
G_PA0	This link selects the gate connector to the BIVOUT0 pin of the AD7293. Inserted: selects BSS159N (R_0 must be populated). Not inserted: BSS159N gate not connected to Loop 0.
S_PA0	This link selects the connection to ground for the amplifier. Inserted: connects the BSS159N source to ground. Not inserted: BSS159N source not connected to Loop 0.
D_PA1	This link selects the drain connector to the BSS159N. Inserted: selects the bottom of the RS1(−) sense resistor. Not inserted: BSS159N drain not connected to Loop 1.
G_PA1	This link selects the gate connector to the BIVOUT1 pin of the AD7293. Inserted: selects BSS159N (R_1 must be populated). Not inserted: BSS159N gate not connected to Loop 1.
S_PA1	This link selects the connection to ground for the amplifier. Inserted: connects the BSS159N source to ground. Not inserted: BSS159N gate not connected to Loop 1.
D_PA2	This link selects the drain connector to the BSS159N. Inserted: selects the bottom of the RS2(−) sense resistor. Not inserted: BSS159N drain not connected to Loop 2.
G_PA2	This link selects the gate connector to the BIVOUT2 pin of the AD7293. Inserted: selects BSS159N (R_2 must be populated). Not inserted: BSS159N gate not connected to Loop 2.

Link Mnemonic	Description
S_PA2	This link selects the connection to ground for the amplifier. Inserted: connects the BSS159N source to ground. Not inserted: BSS159N source not connected to Loop 2.
D_PA3	This link selects the drain connector to the BSS159N. Inserted: selects the bottom of the RS3(−) sense resistor. Not inserted: BSS159N drain not connected to Loop 3.
G_PA3	This link selects the gate connector to the BIVOUT3 pin of the AD7293. Inserted: selects BSS159N (R_3 must be populated). Not inserted: BSS159N gate not connected to Loop 3.
S_PA3	This link selects the connection to ground for the amplifier. Inserted: connects the BSS159N source to ground. Not inserted: BSS159N source not connected to Loop 3.

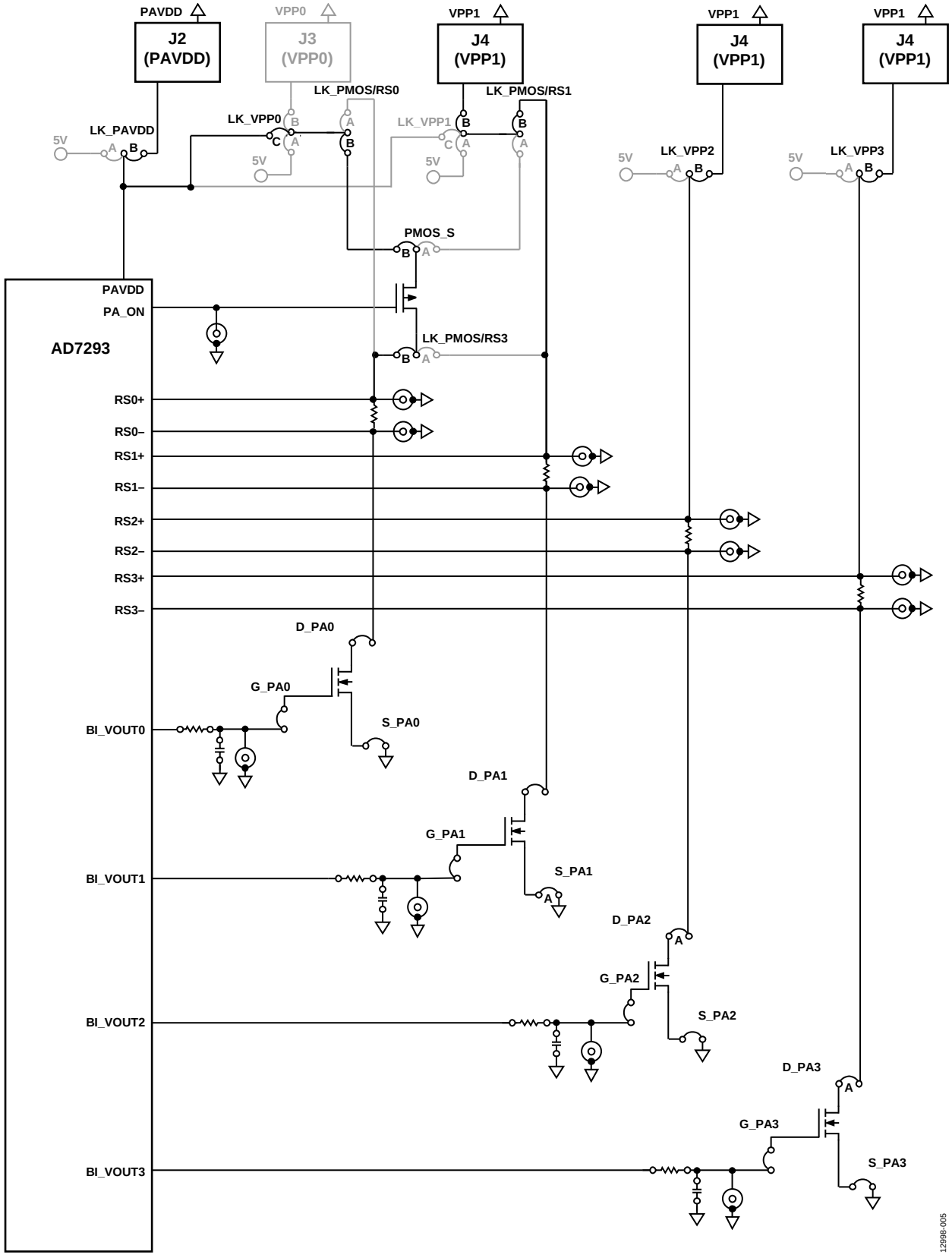


Figure 5. Loop Power Configuration Using On-Board BSS159 Depletion Mode Transistor (Loop 0 with High-Side PMOS Protection)

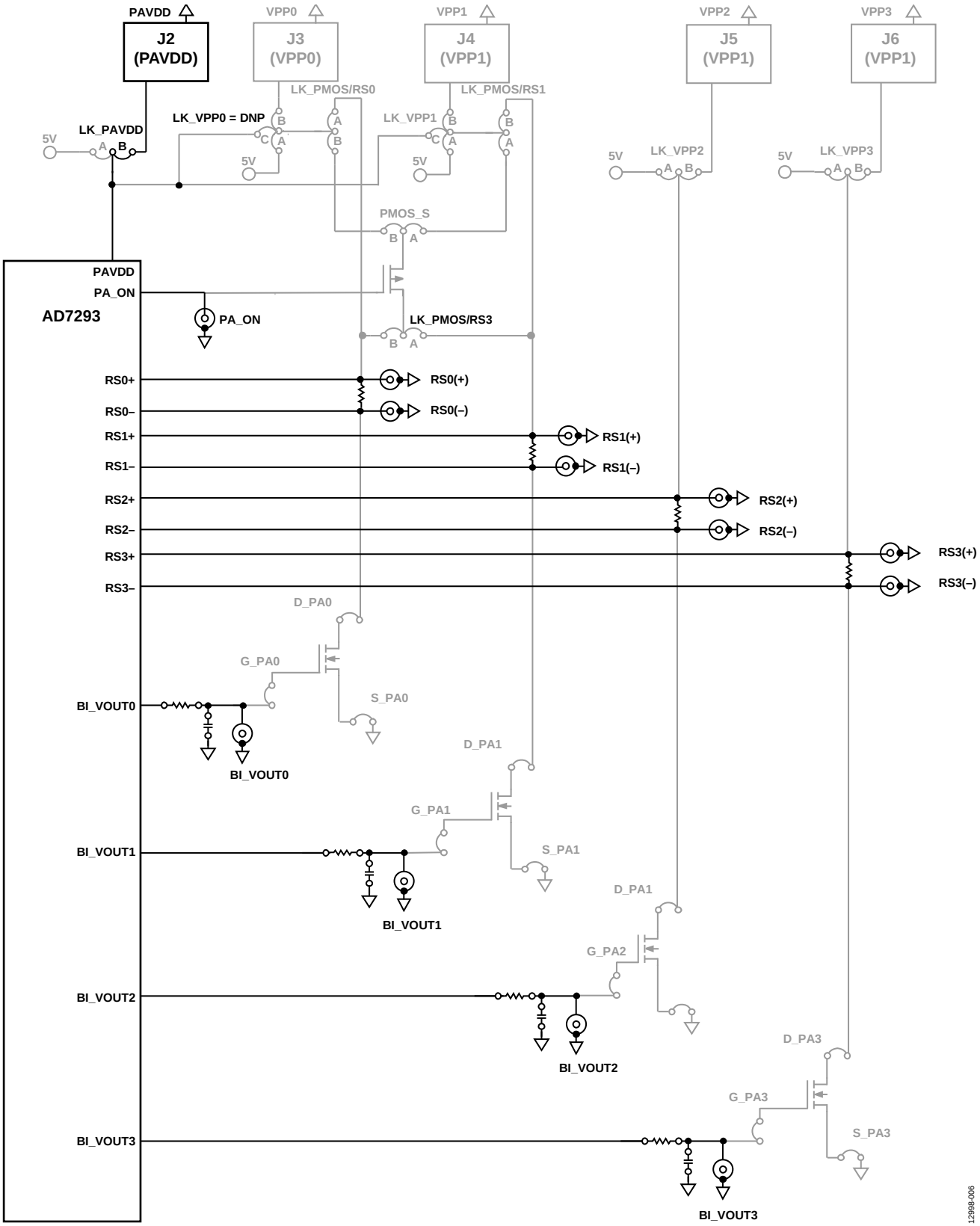


Figure 6. Loop Power Configuration Connecting to External Power Amplifier

ADC INPUT LINKS

The EVAL-AD7293SDZ contains an ADC input channel, including the AD8022 amplifier, to buffer the inputs to the ADC. There are different options available that can be configured using the various links. See Figure 31 and Table 7 for more information.

EXTERNAL REFERENCE LINKS

These links allow the user to select the on-board reference or an external reference.

TEMPERATURE SENSOR LINKS

Three different options are available for use as the input to the AD7293 external temperature sensor:

- A 2NJ906 external diode
- A 2NJ904 external diode (default)
- The D0x or D1x SMB input

See Table 8 for information on how to configure the external temperature sensor using the various links.

Table 7. ADC Input Links

Link Mnemonic	Description
LK_VIN0	Connects the noninverting input of the AD8022 and the VINO SMB to GND.
SL-IN0	Selects the input to the VIN0 pin. Position A: output of the AD8022 op amp. Position B: VINO SMB.
LK_VIN1	Connects the noninverting input of the AD8022 and the VIN1 SMB to GND.
SL-IN1	Selects the input to the VIN1 pin. Position A: output of the AD8022 op amp. Position B: VIN1 SMB.
LK_VIN2	Connects the noninverting input of the AD8022 and the VIN2 SMB to GND.
SL-IN2	Selects the input to the VIN0 pin. Position A: output of the AD8022 op amp. Position B: VIN2 SMB.
LK_VIN3	Connects the noninverting input of the AD8022 and the VIN3 SMB to GND.
SL-IN3	Selects the input to the VIN0 pin. Position A: output of the AD8022 op amp. Position B: VIN3 SMB.

Table 8. Temperature Sensor Links

Link Mnemonic	Description
SLK1	SLK1 and SLK2 determine the use of the D0x SMB, a 2NJ906 or a 2NJ904 external diode, as inputs to the external temperature inputs, D0− and D0+, on the AD7293. Position A: 2NJ906. Position B: 2NJ904 (default). Position C: D0x SMB.
SLK2	SLK1 and SLK2 determine the use of the D0x SMB, a 2NJ906, or a 2NJ904 external diode as inputs to the external temperature inputs, D0− and D0+, on the AD7293. Position A: 2NJ906. Position B: 2NJ904 (default). Position C: D0x SMB.
SLK3	SLK3 and SLK4 determine the use of the D1x SMB, a 2NJ906 or a 2NJ904 external diode, as inputs to the external temperature inputs, D1− and D1+, on the AD7293. Position A: 2NJ906. Position B: 2NJ904 (default). Position C: D1x SMB.
SLK4	SLK3 and SLK4 determine the use of the D1x SMB, a 2NJ906 or a 2NJ904 external diode, as inputs to the external temperature inputs, D1− and D1+, on the AD7293. Position A: 2NJ906. Position B: 2NJ904 (default). Position C: D1x SMB.

Table 9. Default Link Positions for the EVAL-AD7293SDZ

Link Mnemonic	Description
5V_EXT	Inserted
5V_REG	Inserted
LK_AVDD	A
LK_DVDD	A
LK_DVDD1	A
D_PA0	Inserted
D_PA1	Inserted
D_PA2	Inserted
D_PA3	Inserted
G_PA0	Inserted
G_PA1	Inserted
G_PA2	Inserted
G_PA3	Inserted
LK_LDAC	A
LK_PAVDD	A
LK_PMOS/RS0	B
LK_PMOS/RS1	B
LK_PMOS/RS3	B
LK_REF	A
LK_RESET	B
LK_RESET/GPIO	B
LK_SDP_PWR	Inserted
LK_SDP_VDRIVE	Inserted
LK_SLEEP0	A
LK_SLEEP1	A
S_PA0	Inserted
S_PA1	Inserted
S_PA2	Inserted
S_PA3	Inserted
LK_VCC	A
LK_VDRIVE	A
LK_VIN0	Inserted
LK_VIN1	Inserted
LK_VIN2	Inserted
LK_VIN3	Inserted
LK_VPP0	C
LK_VPP1	B
LK_VPP2	B
LK_VPP3	B
LK_VSS	A
PMOS_S	B
SL-IN0	A
SL-IN1	A
SL-IN2	A
SL-IN3	A
SLEEP0	Inserted
SLEEP1	Inserted
SLK1	B
SLK2	B
SLK3	B
SLK4	B

SOCKETS

There are 23 SMB input/output sockets on the EVAL-AD7293SDZ that are relevant to the operation of the AD7293. These sockets apply an externally generated signal to the EVAL-AD7293SDZ for connecting an external circuit to the EVAL-AD7293SDZ or for accessing an output signal from the AD7293.

Table 10. Socket Functions

Socket Mnemonic	Description
RS0(+), RS1(+), RS2(+), RS3(+), RS0(–), RS1(–), RS2(–), RS3(–)	Subminiature bayonet nut connector (BNC) sockets for the input signals applied directly to the RSx+ and RSx– inputs in the absence of a sense resistor.
VIN0, VIN1, VIN2, VIN3	Subminiature BNC sockets for the analog input signals applied directly to the VIN0, VIN1, VIN2, and VIN3 pins, respectively.
D0x, D1x	Subminiature BNC sockets for the input signals applied directly to the AD7293 D0± and D1± pins.
PA_ON	Subminiature BNC sockets for the PA_ON output signal generated by the AD7293.
UNI_VOUT0, UNI_VOUT1, UNI_VOUT2, UNI_VOUT3, BI_VOUT0, BI_VOUT1, BI_VOUT2, BI_VOUT3	Subminiature BNC sockets for the $V_{OUT}x$ output signals generated by the AD7293.

GETTING STARTED

INSTALLING THE SOFTWARE

The EVAL-AD7293SDZ evaluation kit CD includes self installing software. The software is compatible with Windows® XP, Windows Vista, and Windows 7. Note that the EVAL-AD7293SDZ interfaces to the USB port of the PC via the EVAL-SDP-CB1Z.

To ensure that the EVAL-SDP-CB1Z is recognized when it connects to the PC, install the software before connecting the EVAL-SDP-CB1Z to the USB port of the PC.

1. Start the Windows operating system and insert the CD.
2. The installation software opens automatically. If it does not open automatically, run the **setup.exe** file from the CD. Install the software as well as any drivers that are prompted.
3. After installation is complete, power up the EVAL-AD7293SDZ as described in the AD7293 Power Supply section.
4. Plug the EVAL-AD7293SDZ into the EVAL-SDP-CB1Z, and plug the EVAL-SDP-CB1Z into the PC using the USB cable included in the box.
5. To finalize the installation, proceed through any dialog boxes that appear when the software detects the EVAL-AD7293SDZ.

OPERATING THE SOFTWARE

To run the AD7293 evaluation software, take the following steps:

1. From the **Start** menu, go to **All Programs**, **Analog Devices**, **AD7293**, and click **AD7293 Evaluation Software**. To uninstall the program, click **Start**, **Control Panel**, **Add or Remove Programs**, and then click **AD7293 Evaluation Software**.
2. Plug the USB cable into the EVAL-SDP-CB1Z, then plug the EVAL-SDP-CB1Z into the EVAL-AD7293SDZ and secure it using plastic screws (see Figure 7).

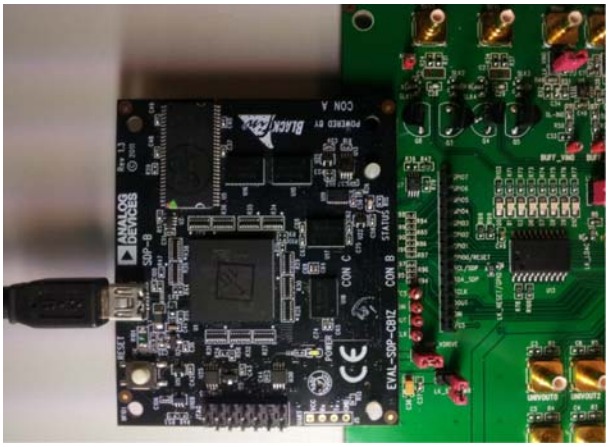


Figure 7. EVAL-AD7293SDZ Connected to the EVAL-SDP-CB1Z

3. If the EVAL-SDP-CB1Z is not connected to the USB port when the software is launched, a connectivity error displays (see Figure 8). Plug the USB cable into the EVAL-SDP-CB1Z, then plug the EVAL-SDP-CB1Z into the EVAL-AD7293SDZ, wait a few seconds, click **Rescan**, and follow the instructions.

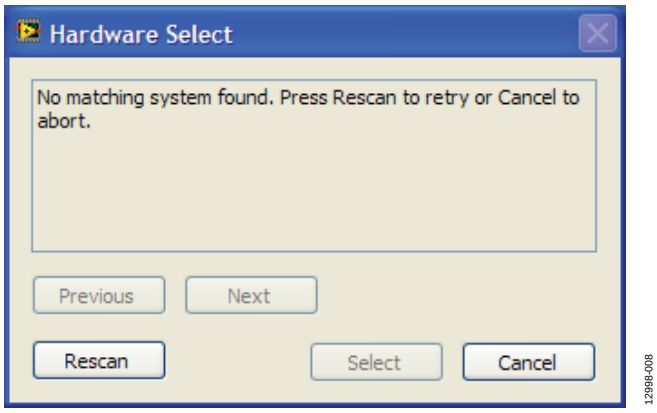


Figure 8. Connectivity Error

4. If the EVAL-SDP-CB1Z is not connected to the EVAL-AD7293SDZ, a message box appears (see Figure 9). Check that the connection between the EVAL-SDP-CB1Z and the EVAL-AD7293SDZ, and run the program again.

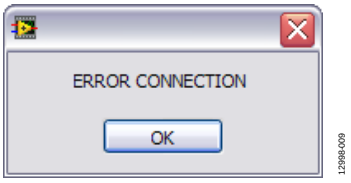


*Figure 9. **ERROR CONNECTION** Window*

5. If the EVAL-SDP-CB1Z is connected, the system development platform connects for a brief period.

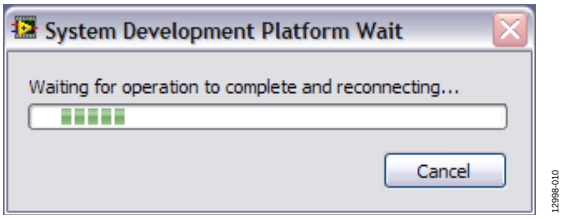


*Figure 10. **System Develop Platform Wait** Window*

6. The main window of the EVAL-AD7293SDZ then opens.
7. After installing the software, remove the CD from the disc drive.

VERIFYING THE LINKS AND POWERING UP THE EVALUATION BOARD

Ensure that all links are positioned correctly for the chosen operating mode. Table 9 shows the position in which all links are set when the EVAL-AD7293SDZ is packaged.

When using an external power supply, follow these steps:

1. Ensure that all links are positioned correctly for the chosen operating mode.
2. Ensure that all relevant external power connections are made before using the software for the device.
3. Plug in the USB cable and the EVAL-SDP-CB1Z. If the supplied software is not used and all external supplies are used, this cable is not required.
4. Turn on the external power supply.

After powering up the EVAL-AD7293SDZ, begin using the software to evaluate the board. Note that the EVAL-AD7293SDZ must be repowered when the software window is closed; that is, the USB must be disconnected and reinserted.

EVALUATING THE BOARD

The EVAL-AD7293SDZ software allows the user to load values to the eight DACs in the AD7293, read values from the ADC channels ,and then depict these values in a plot, monitor a signal between two limited values, and change the configuration of the device.

USING THE SOFTWARE

AD7293 EVALUATION BOARD SOFTWARE WINDOW

After following the procedures in the Getting Started section, the **AD7293 Evaluation Board Software** window, shown in Figure 11, appears when the evaluation software program is started. A number of different tabs are available to navigate through the various operating functions of the EVAL-AD7293SDZ. Click the relevant tab to select the various modes and configurations of the device.

The tabs offer the following options:

- **System View**
- **Hardware Pins**
- **ADC Monitoring**
- **Temperature Sensing**
- **Current Sensing**
- **DAC Control**
- **Closed Loop**
- **Access Register**
- **GPIOs/Alerts**

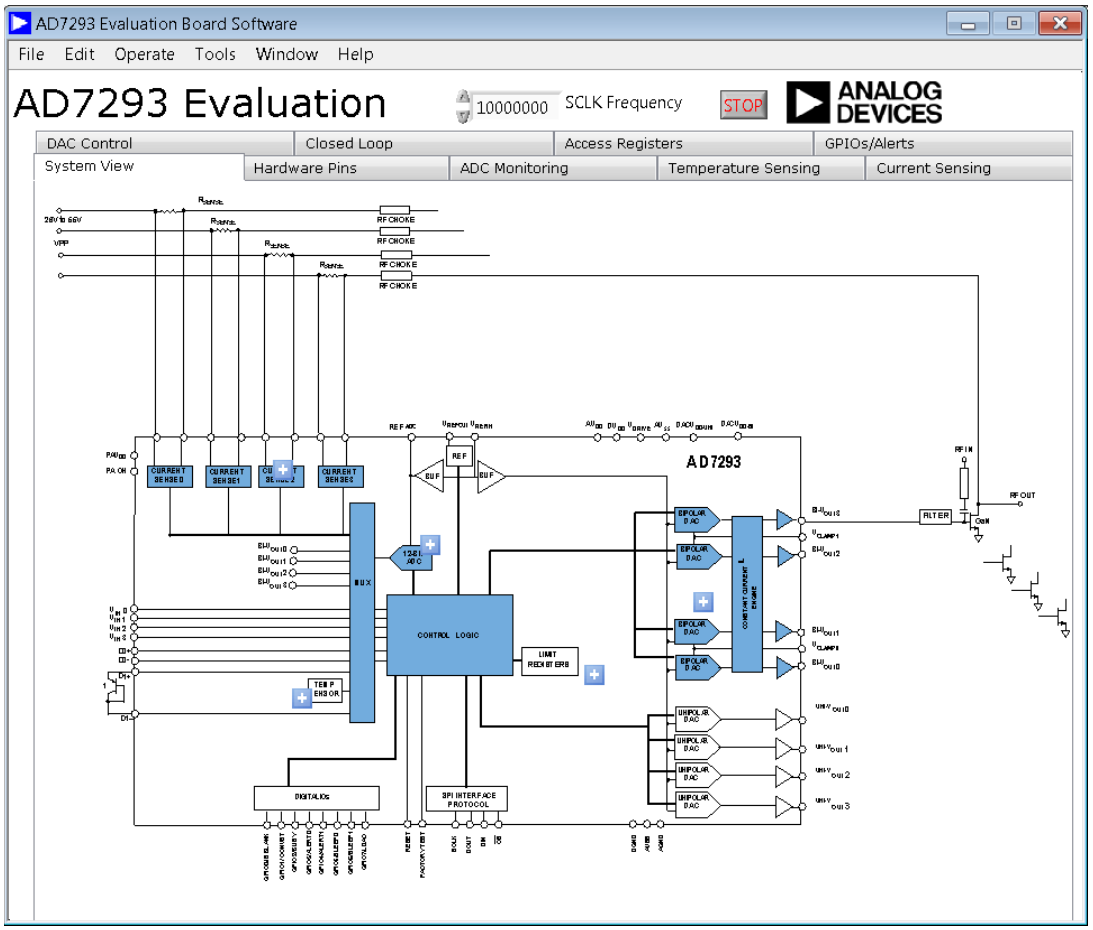


*Figure 11. **AD7293 Evaluation Board Software** Window*

HARDWARE PINS

Four hardware pins are configurable from the **Hardware Pins** tab. The hardware pins are $\overline{\text{LDAC}}$, $\overline{\text{RESET}}$, SLEEP0, and SLEEP1. The links on the EVAL-AD7293SDZ must be configured as shown in Figure 12 to work accordingly.

$\overline{\text{LDAC}}$ and $\overline{\text{RESET}}$ are active low inputs. To use the pins, the user must set the corresponding switch to either high or low and then click **Write to SDP**.

Consult the AD7293 data sheet for more information on the function of the pins.

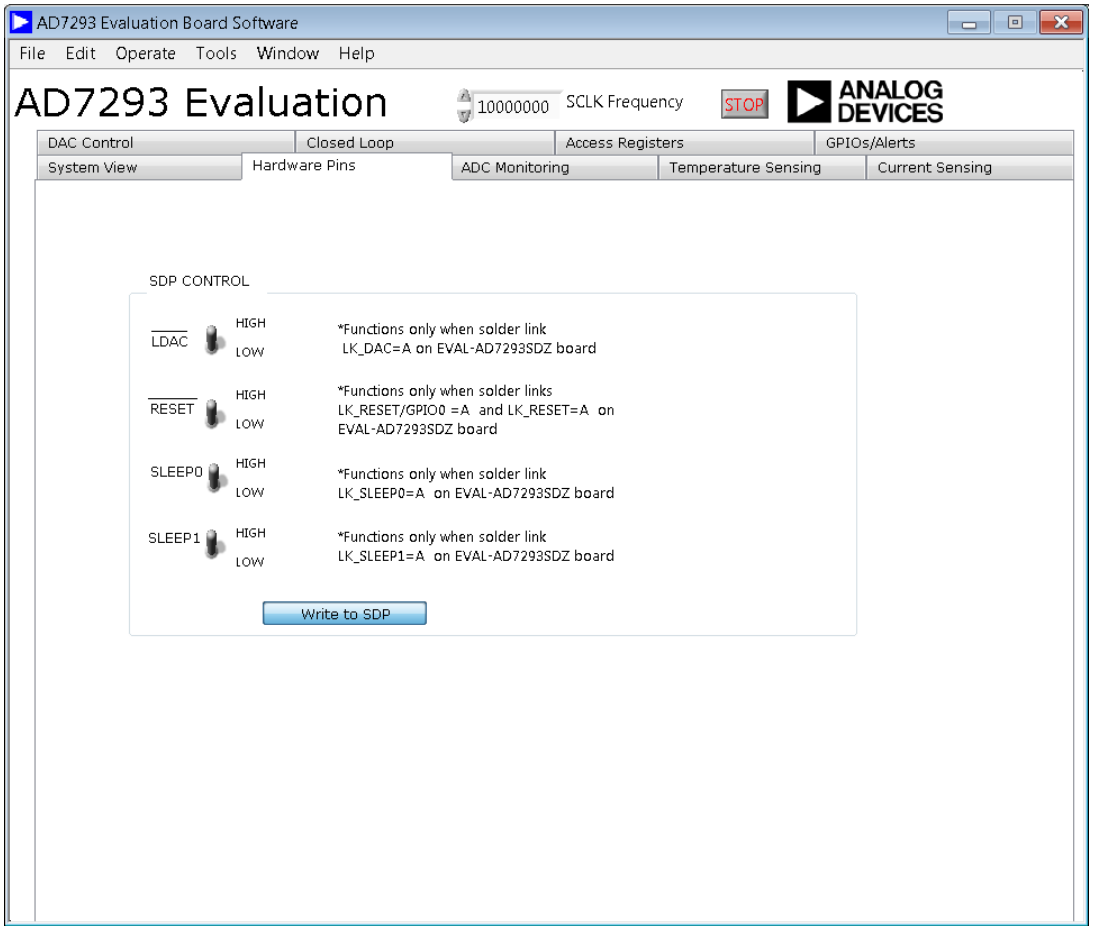


*Figure 12. **Hardware Pins** Tab*

ADC MONITORING TAB

To read the converted analog signals from the 4-channel ADC, click **Sample** in the **ADC Monitoring** tab of the main window. This tab allows the user to make single-ended measurements on the ADC channels.

The **Continuous OFF/ON** box allows the user to make continuous measurements in command mode. Within the **ADC Monitoring** tab, use the **Vin 0**, **Vin 1**, **Vin 2**, and **Vin 3** boxes to select the channel accessed. To read the converted data, click **Sample** to add one value at a time to a display box, or select **Continuous OFF/ON** to store the values in an array to draw the scope plot. Various user options are also available in this window, such as range settings and offset settings (see Figure 13).

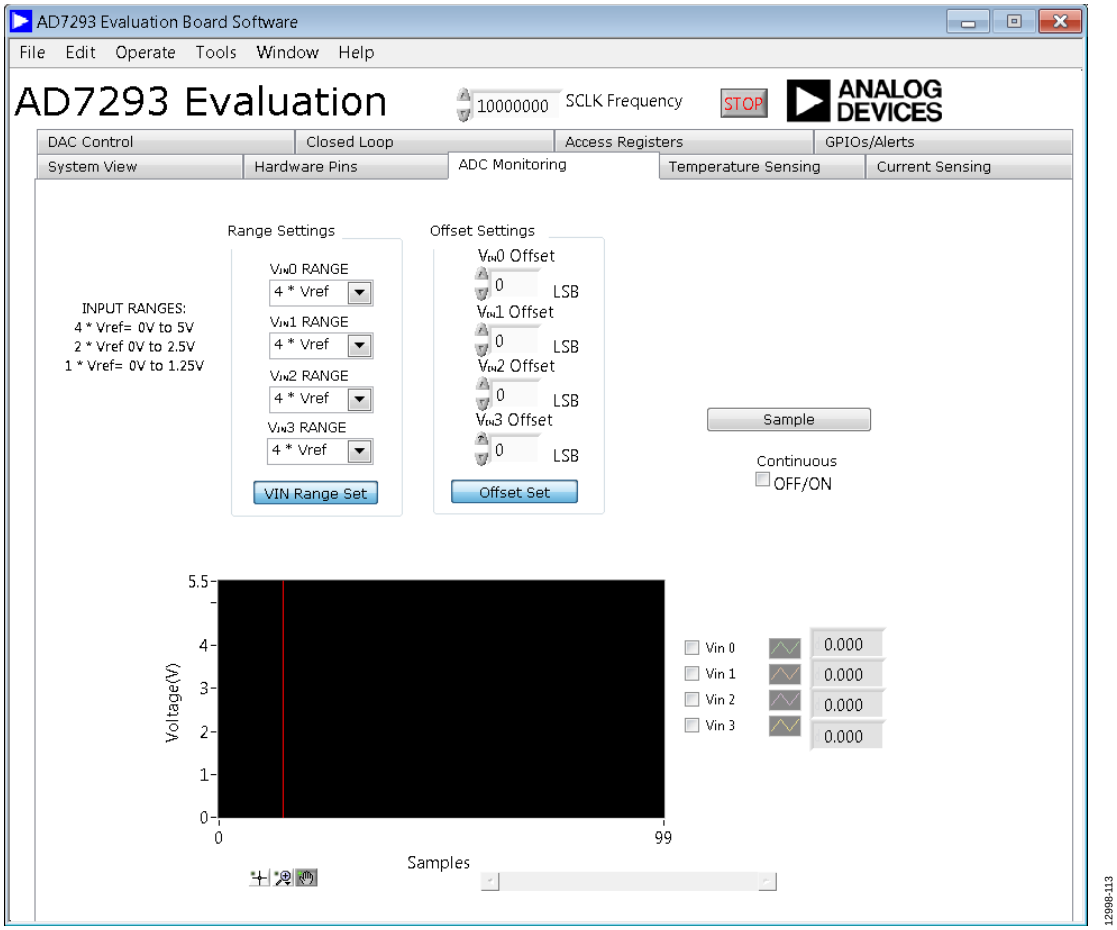


*Figure 13. **ADC Monitoring** Tab*

TEMPERATURE SENSING TAB

To read the temperature from the AD7293, click **Sample** in the **Temperature Sensing** tab of the main window. The **Continuous OFF/ON** box allows the user to make continuous measurements in command mode. Within the **Temperature Sensing** tab, use the **Tsense 1**, **Tsense 2**, and **Tsense INT** check boxes to select the channel accessed. To read the converted data, click **Sample** to add one value at a time to a display box, or select **Continuous OFF/ON** to store the values in an array to draw the scope plot. **Tsense Offset Settings** are also available in this tab.

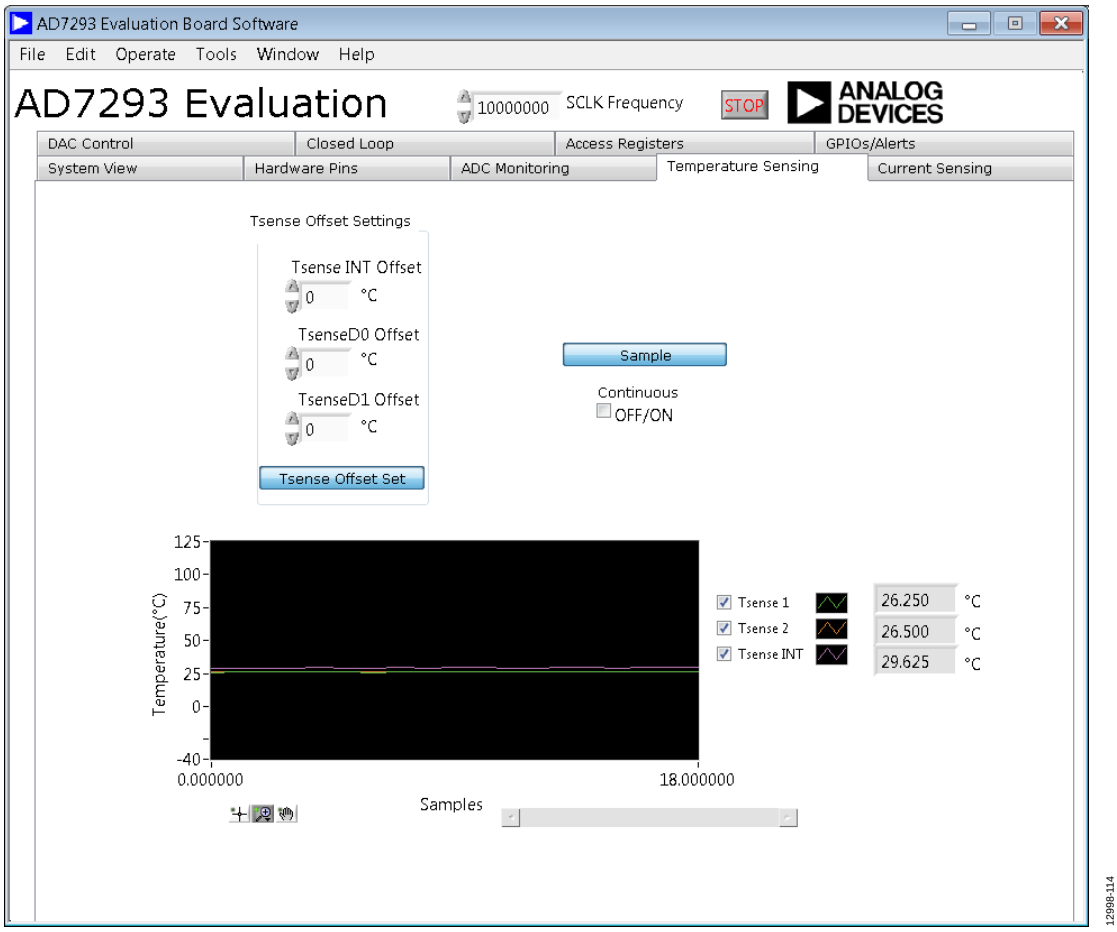


*Figure 14. **Temperature Sensing** Tab*

CURRENT SENSING TAB

To read the converted analog signals from the four current sense channels, click **Sample** in the **Current Sensing** tab of the main window. The **Continuous OFF/ON** box allows the user to make continuous measurements in command mode. Checking the **Isense 0** to **Isense 3** boxes allows the user to select which channel is accessed. There are two methods of reading the converted data: click **Sample** to add one value at a time to a display box, or click **Continuous OFF/ON** to store the values in an array to draw the scope plot. Various user options are also available in this window, such as ISENSE gain and offset settings (see Figure 15).

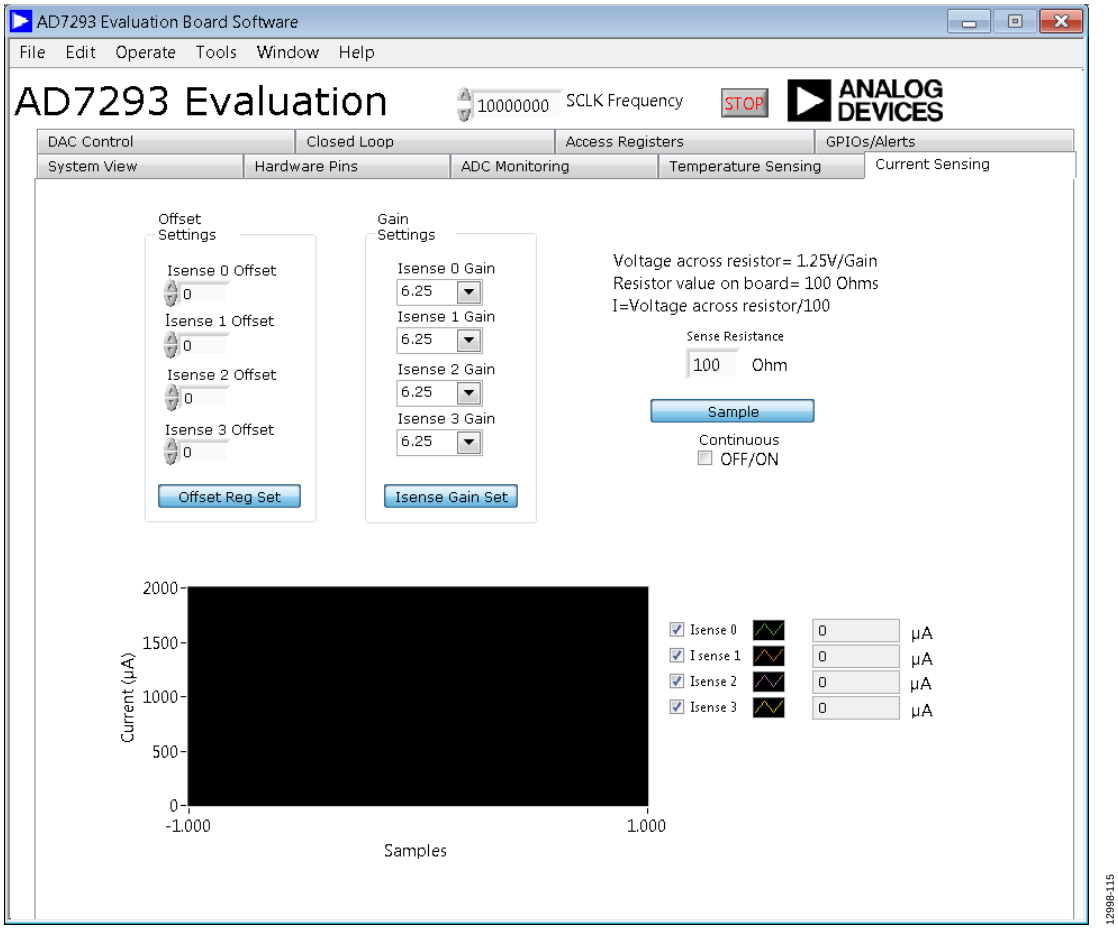


*Figure 15. **Current Sensing** Tab*

DAC CONTROL TAB

The **DAC Control** tab in the main window allows the user to select any of the eight DAC outputs and then load a value, using the **DAC CODE** box (see Figure 16). The write is dependent on the $\overline{\text{LDAC}}$ pin when **LOAD** is selected. If left unselected, the DAC loads when **Write to DAC** is clicked. If **COPY** is selected, the value is copied to all relevant DAC channels (unipolar or bipolar depending on which DAC is selected).

Use the **Enable Channels** boxes to select which channels are enabled when **Write to DAC** is clicked.

To select the DAC output range setting, go to the drop-down menu in the relevant channel, make a selection, and then click **DAC Offset Set**.

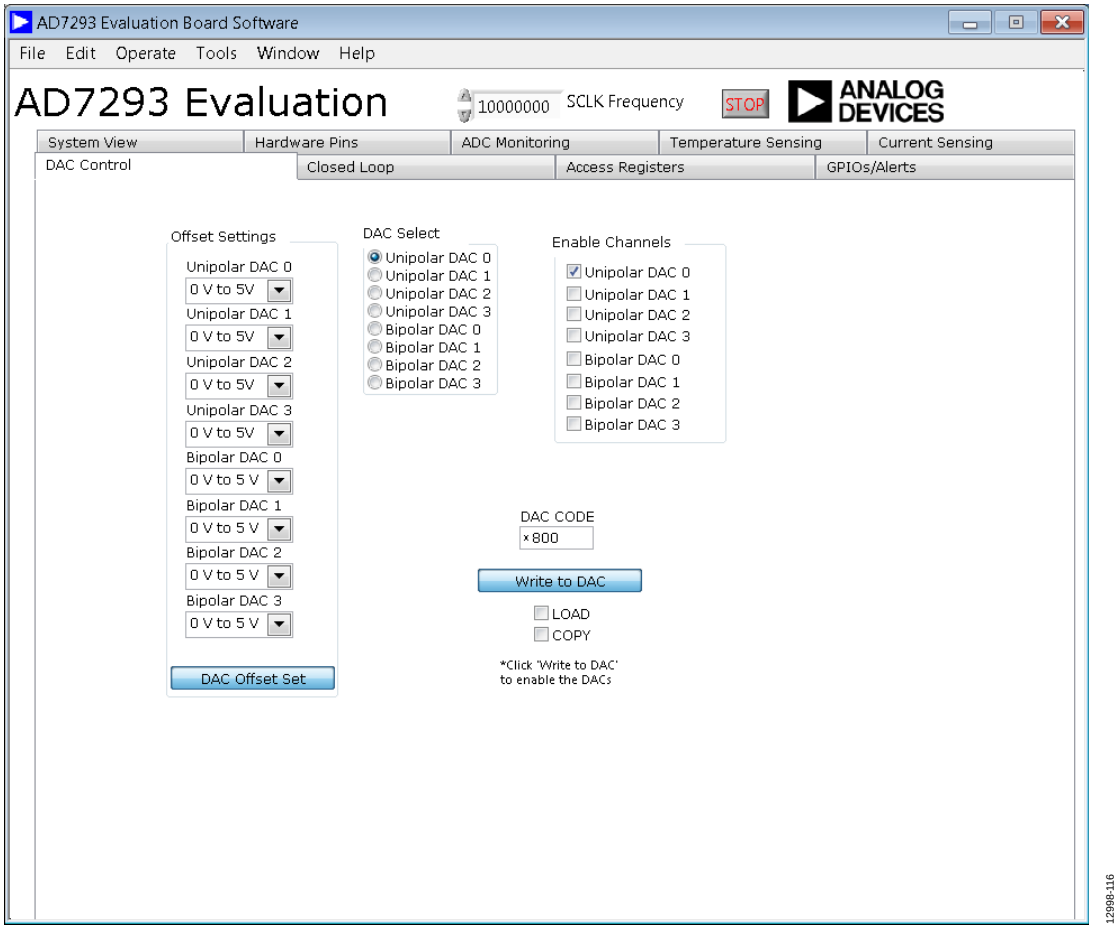


*Figure 16. **DAC Control** Tab*

CLOSED LOOP TAB

Use the **Closed Loop** tab to control Loop 0 of the EVAL-AD7293SDZ. Use **STEP 1A**, **STEP 1B**, **STEP 2**, and **STEP 3** (see Figure 17 and Figure 18) to set up the AD7293 for closed-loop operation:

- **STEP 1A** allows the user to enable the loop.
- **STEP 1B** controls the external PMOS switch on the EVAL-AD7293SDZ via the PA_ON circuitry on the AD7293. Check off the **PA_ON state on/off?** box to turn the supply to the top of the sense resistor on or off, allowing current to flow to the rest of the circuit.

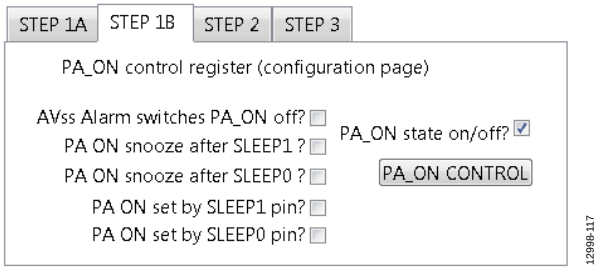


*Figure 17. **STEP 1B** Tab*

- **STEP 2** allows the user to write the target current by writing to the DAC register.
- **STEP 3** allows the user to enable Bipolar DAC 0, the DAC that controls the gate of the transistor in Loop 0.

The user can also program the target current and ramp time. Click **MEASURE CURRENT, VOLTAGE & SET HIGH LIMIT** to measure the current at the current sense input (see Figure 18). This button also measures the DAC output voltage and sets the high alert limit on the AD7293. Select the **Continuous OFF/ON** box to allow continuous measurements in command mode.

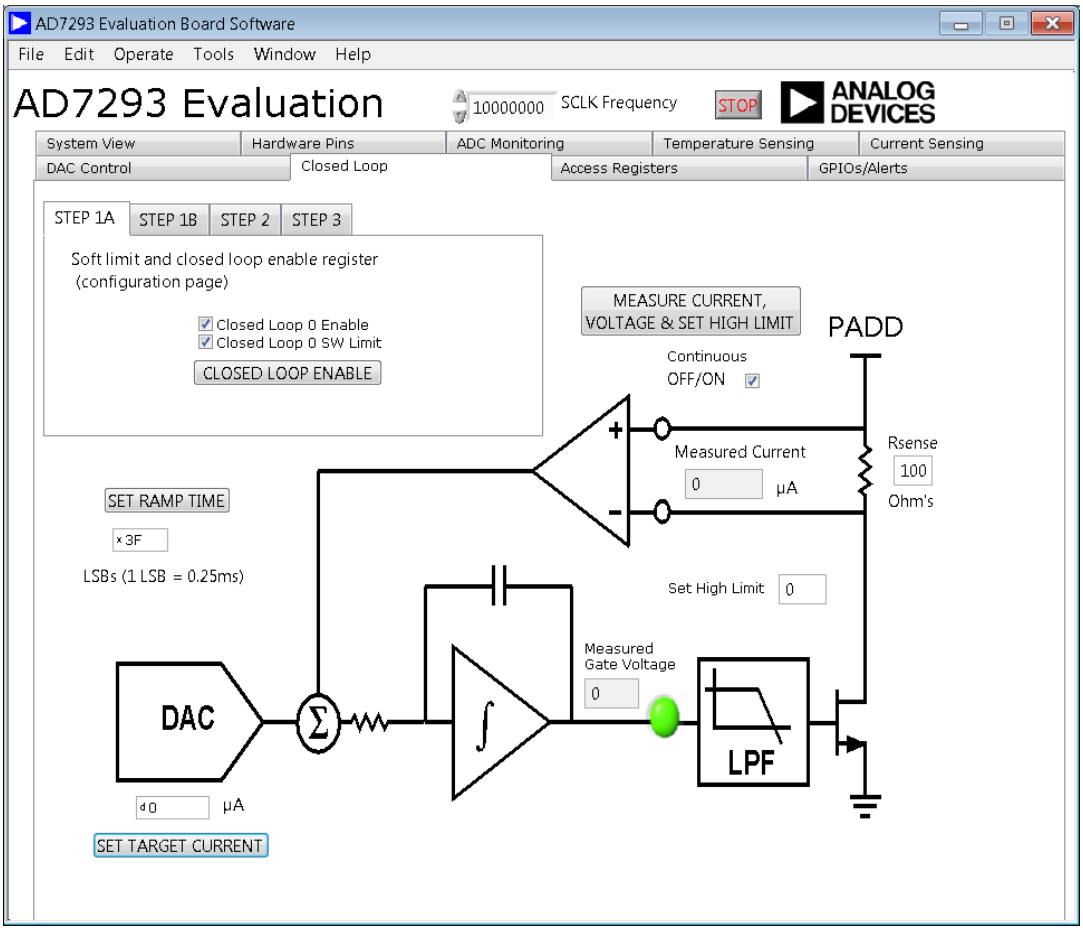


*Figure 18. **Closed Loop** Tab*

AD7293 REGISTER INTERFACE WINDOW

In the **Access Registers** tab, click **Access All Registers** to navigate to the AD7293 **Register Interface** window (see Figure 19). This window allows access to all registers.

In the left column, select the page under **Page Selector**. In the **Register Selector** column, select the register. Use the **Register** column (shown in the center of Figure 19) to select the data being written to the register. Enter the value in the text box directly under **Register** or click the relevant bit. Drop-down menus or text boxes appear when appropriate.

Click **Write** to perform a write to the register in use.

Click **Read** to read the register contents.

Click **Reset to default** to reset the register value to the software default. Note that clicking this does not write to the device.

Click **Search** to search for a phrase. For example, enter **DAC** to pull up all registers with DAC in the title.

The **i** icon displays further details on the function of the register.

Click **Log>>** to enlarge or shrink the window to include the **Communications Log**.

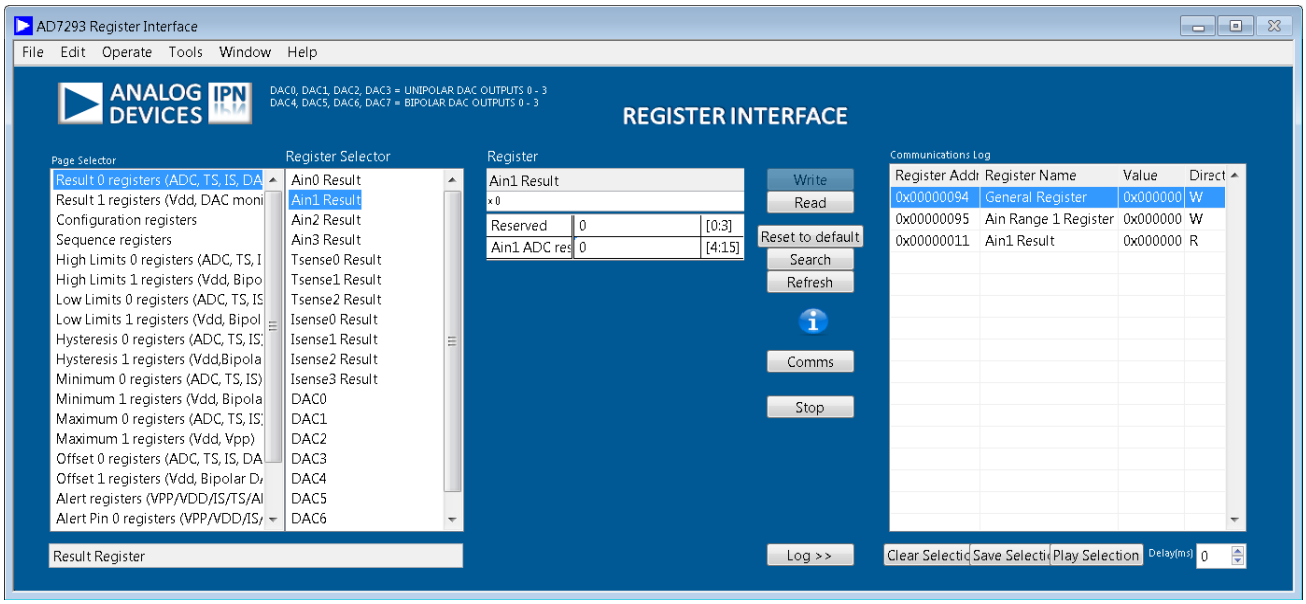


*Figure 19. **AD7293 Register Interface** Window*

COMMUNICATIONS LOG

The **Communications Log** panel allows the user to play patterns and display the writes or reads made to the device. Use the standard windows highlighting commands to repeat a pattern or a selection of writes and reads from the communications log. Figure 20 shows three items displayed in the communications log. Click **Play Selection** to play these patterns.

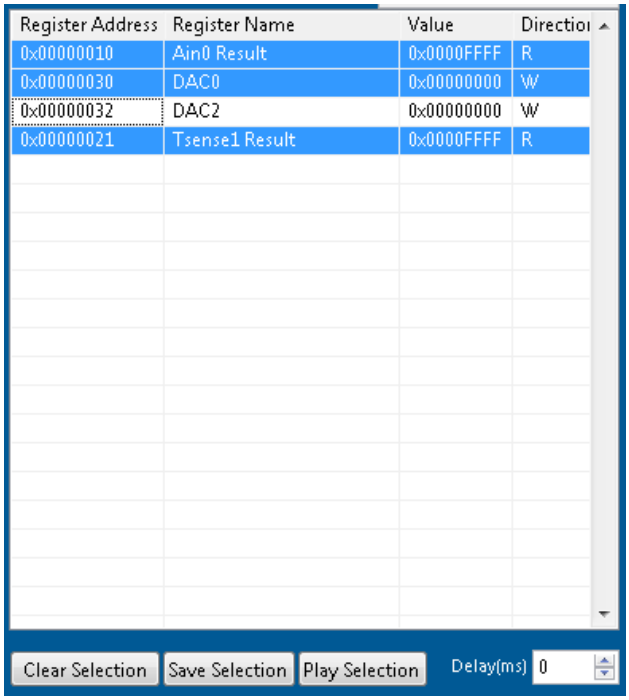


*Figure 20. **Communications Log** Before Clicking **Play Selection***

Figure 21 shows the **Communications Log** after clicking **Play Selection**.

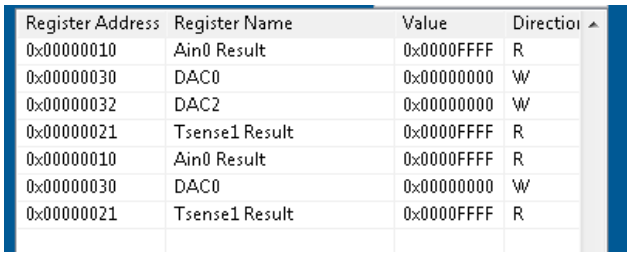


*Figure 21. **Communications Log** After Clicking **Play Selection***

Click **Save Selection** to save the file. Use a .txt extension when saving the file (see Figure 20 and Figure 22).

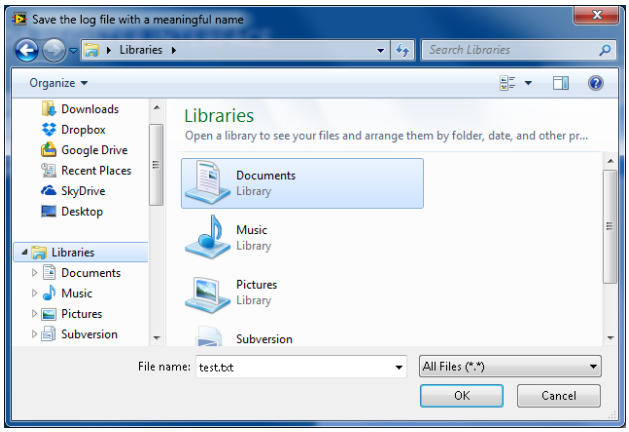


*Figure 22. **Save Selection** Window*

To play the sequence at a later point, click **Comms Log** from the drop-down menu and then click **Play From File** (see Figure 23). Select the saved file and click **OK** to play the previously saved pattern.

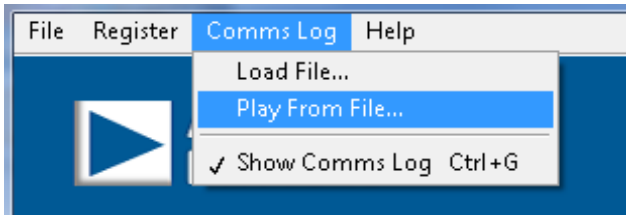


Figure 23. Play Previously Saved Selection

GPIOs/ALERTS TAB

Use the **GPIOs/Alerts** tab to control the pin functions of the EVAL-AD7293SDZ. See Figure 24 for the **GPIOs/Alerts** tab. Each pin has a dual function and is configurable by clicking the relevant button (for example, the **GPIO0** button) in the top row. See the AD7293 data sheet for the pin functions. The **INPUT/OUTPUT** button on the second row configures the pin for input or output. When **INPUT** is selected, the third row indicates the state of the pin. When **OUTPUT** is selected, the user can configure the output as low or high by clicking **LOW/HIGH** in the third row.

The fourth row of buttons decides the polarity (active high or active low) of the pin when the pin is not configured for GPIO. See Table 11 for a list of the available software configurations.

The user can set the upper and lower limits on the alerts listed. Enter the required limits, select the **Enable** box on the alert, and then click **Write Alerts**. To view the alerts status, click **Read Alerts**.

The alerts can also be routed to either the ALERT0 pin or the ALERT1 pin. Either the high or low limit or both limits on each alert can be configured to activate the relevant alert pin. Click the relevant limits to be routed, and then click **Route Alerts to pins**.

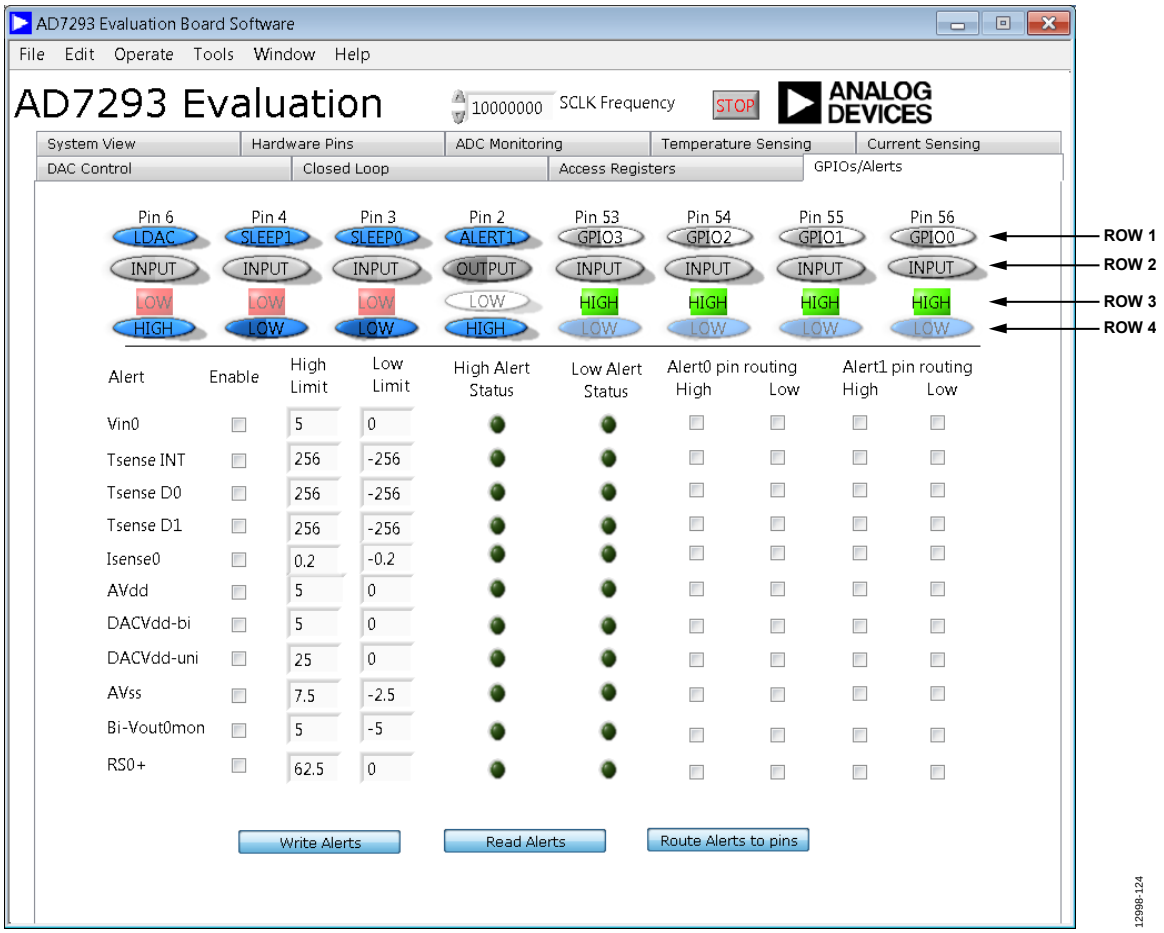


*Figure 24. **GPIOs/Alerts** Tab*

Table 11. GPIO Configurations

Function	Row 1	Row 2	Row 3	Row 4
Input	GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7	INPUT	LOW/HIGH (current pin)	Not applicable
Output	GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7	OUTPUT	LOW/HIGH (output state)	Not applicable
Alternate Function	IS BLANK, CONVST, BUSY, ALERT0, ALERT1, SLEEP0, SLEEP1, LDAC	Not applicable	LOW/HIGH (current pin)	HIGH/LOW (active polarity)

EVALUATION BOARD SCHEMATICS AND ARTWORK

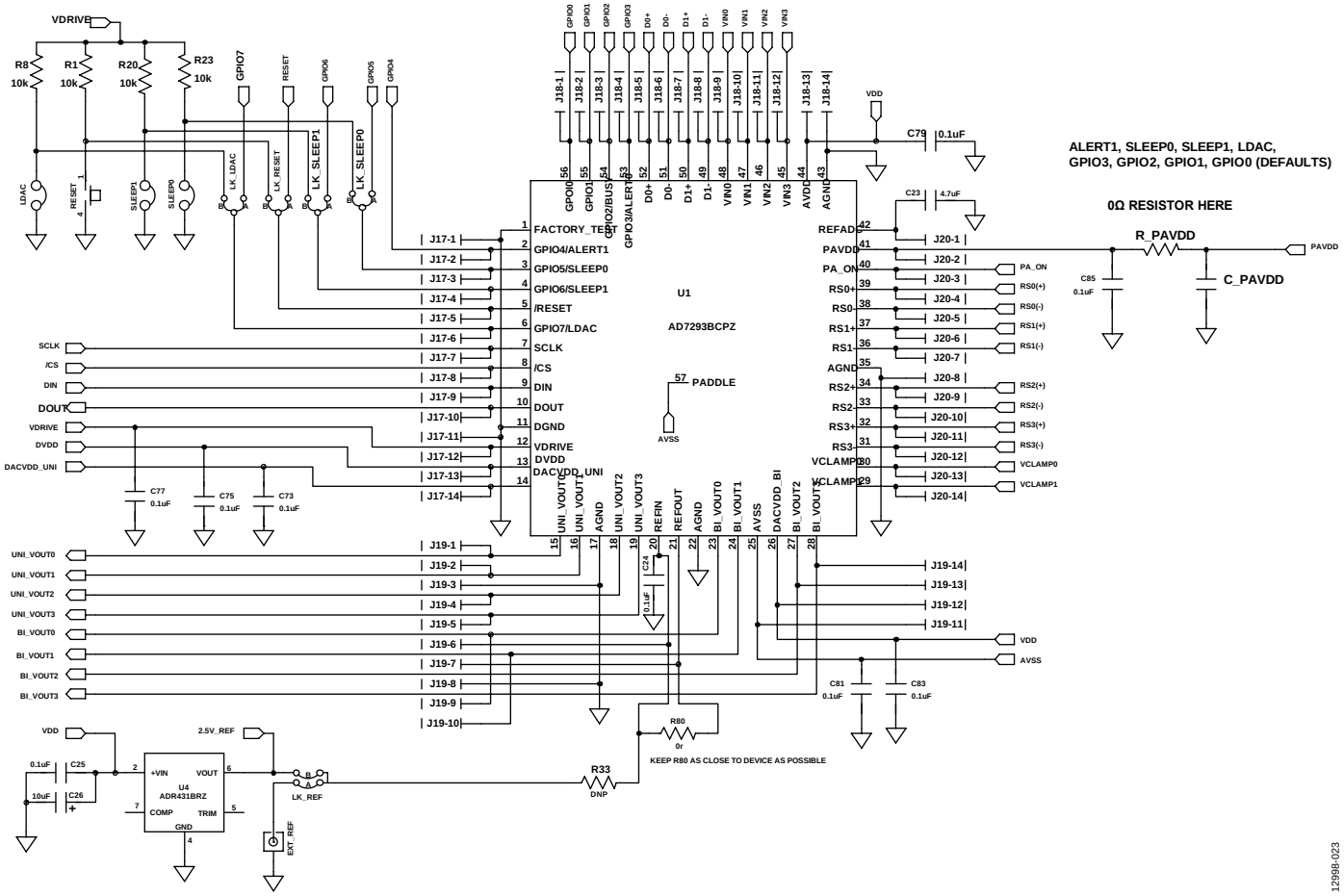


Figure 25. EVAL-AD7293SDZ Schematic, AD7293 Block

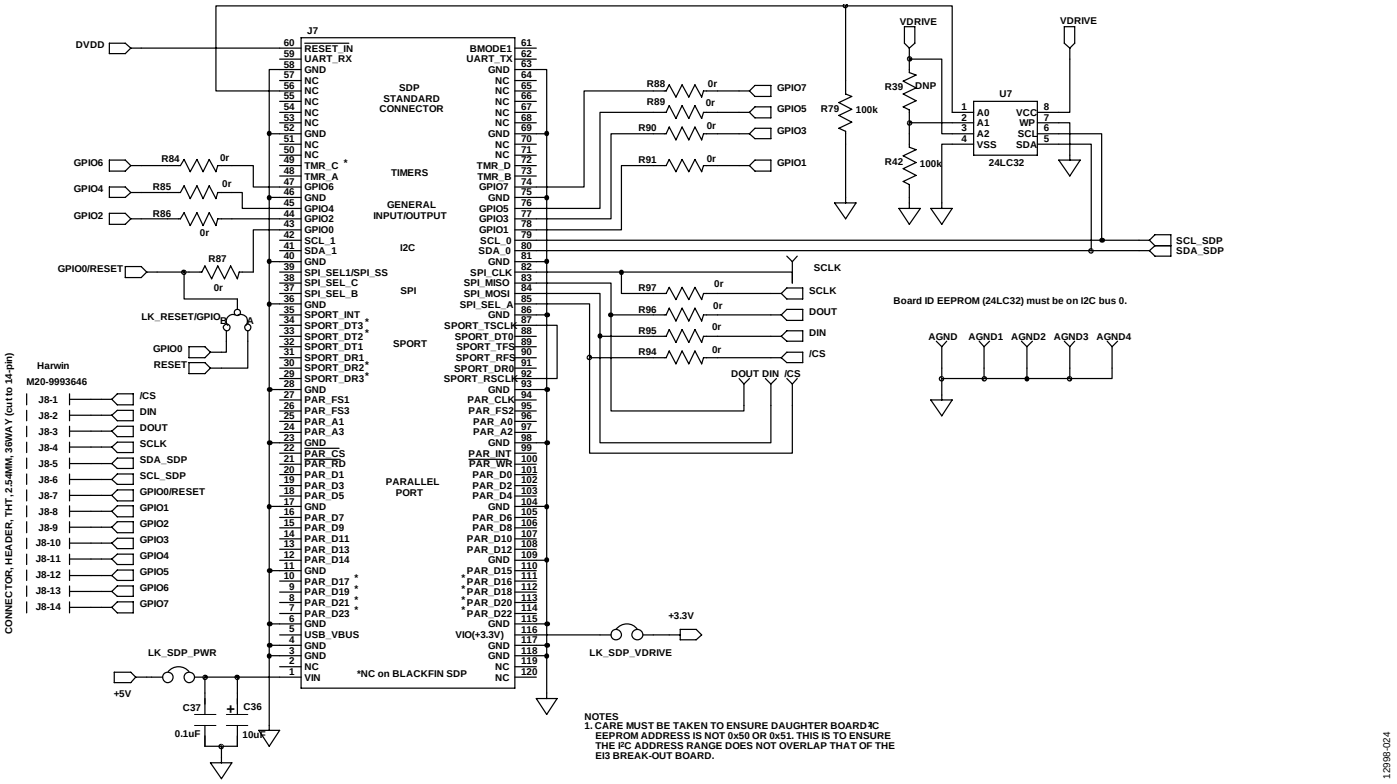


Figure 26. EVAL-AD7293SDZ Schematic, SDP Connector Block

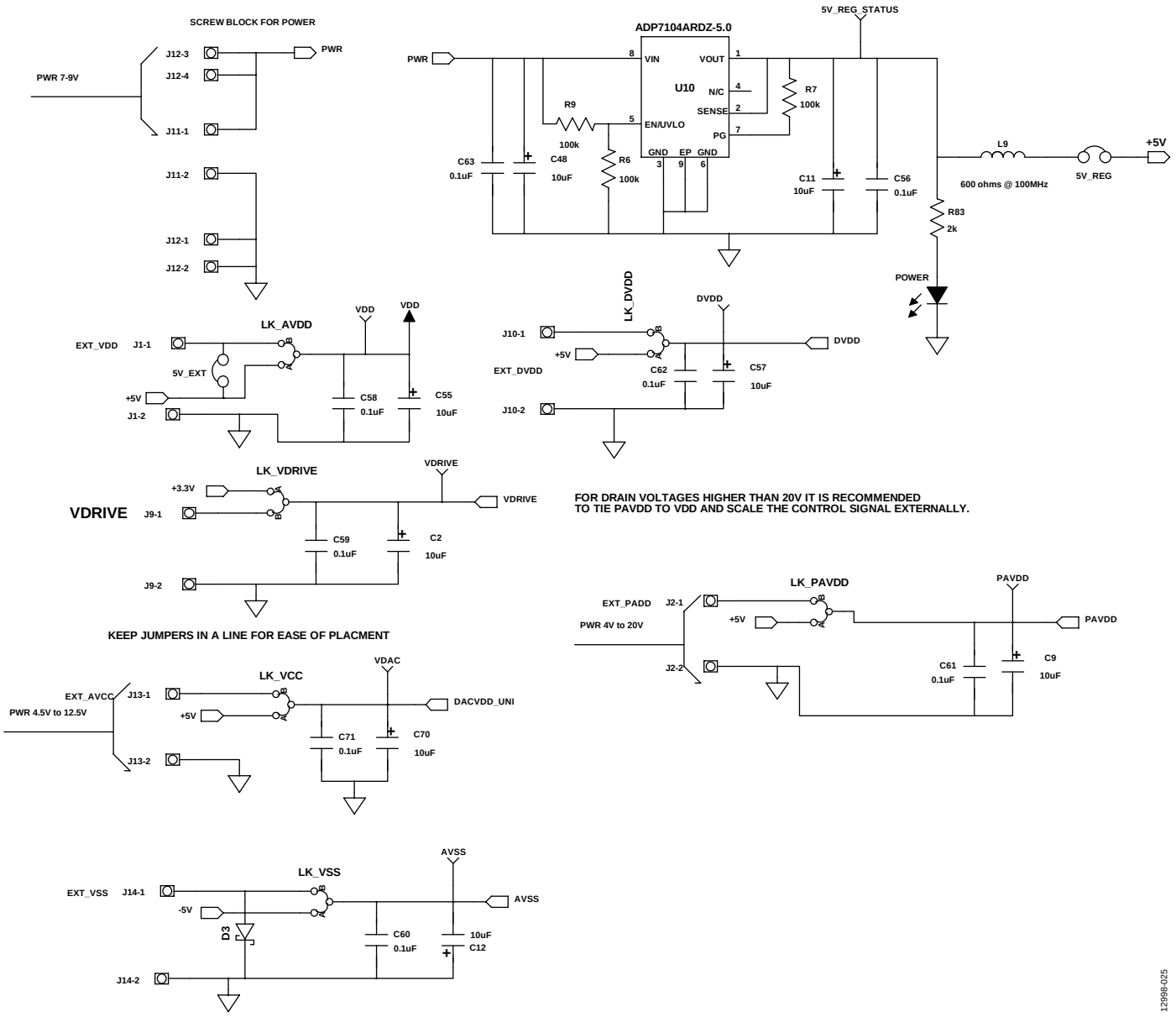


Figure 27. EVAL-AD7293SDZ Schematic, Power Supply Block

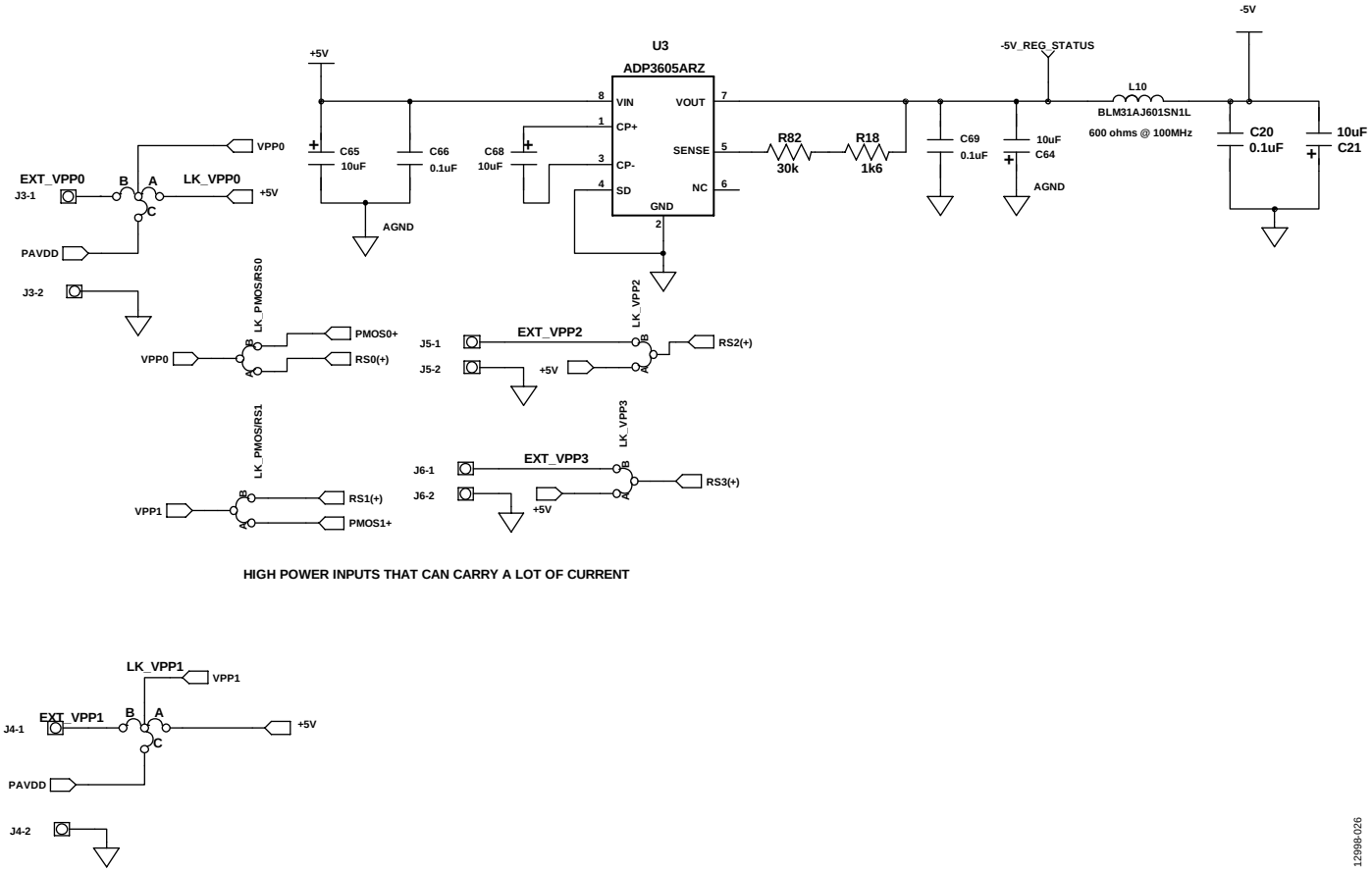


Figure 28. EVAL-AD7293SDZ Schematic, VPP and Negative Power Supply Block

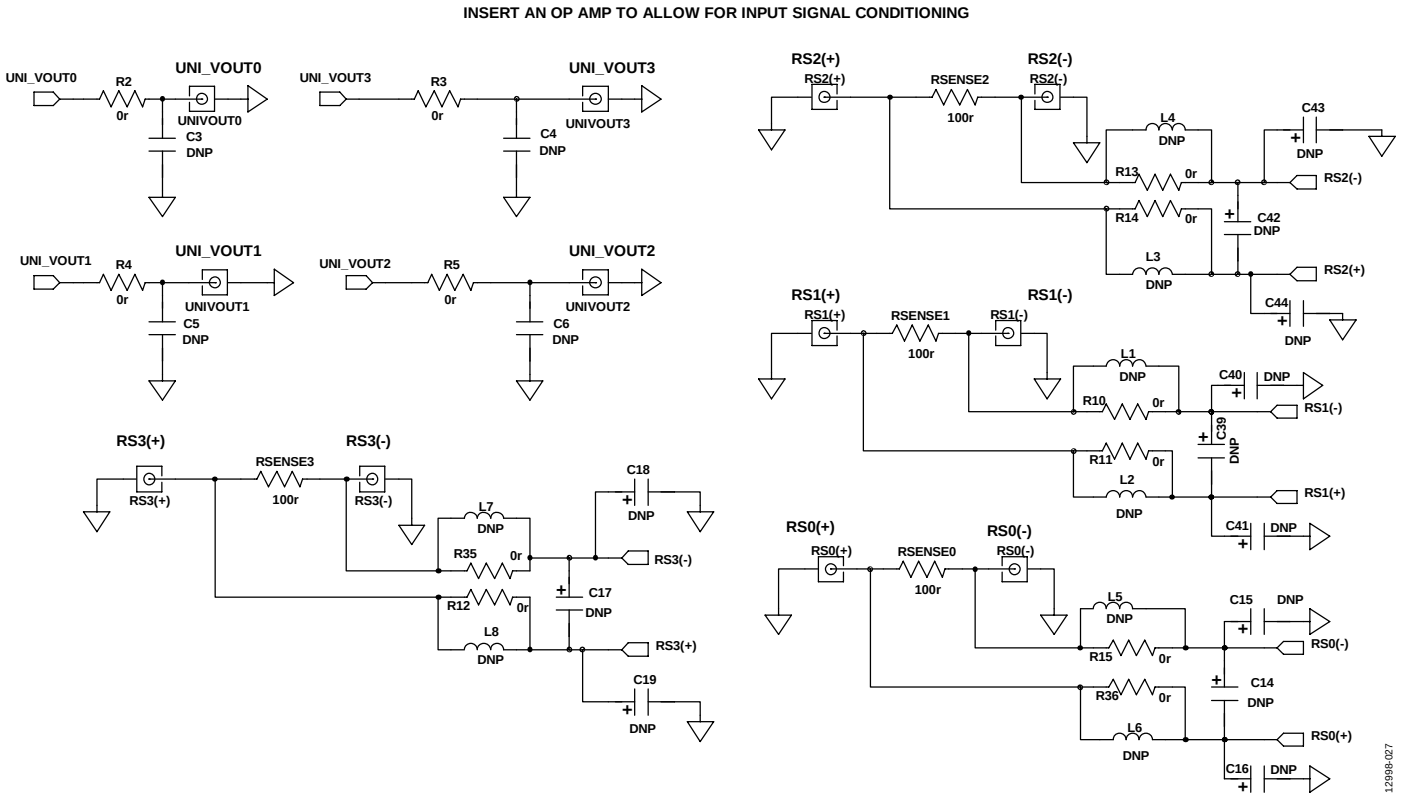


Figure 29. EVAL-AD7293SDZ Schematic, Current Sensors Block

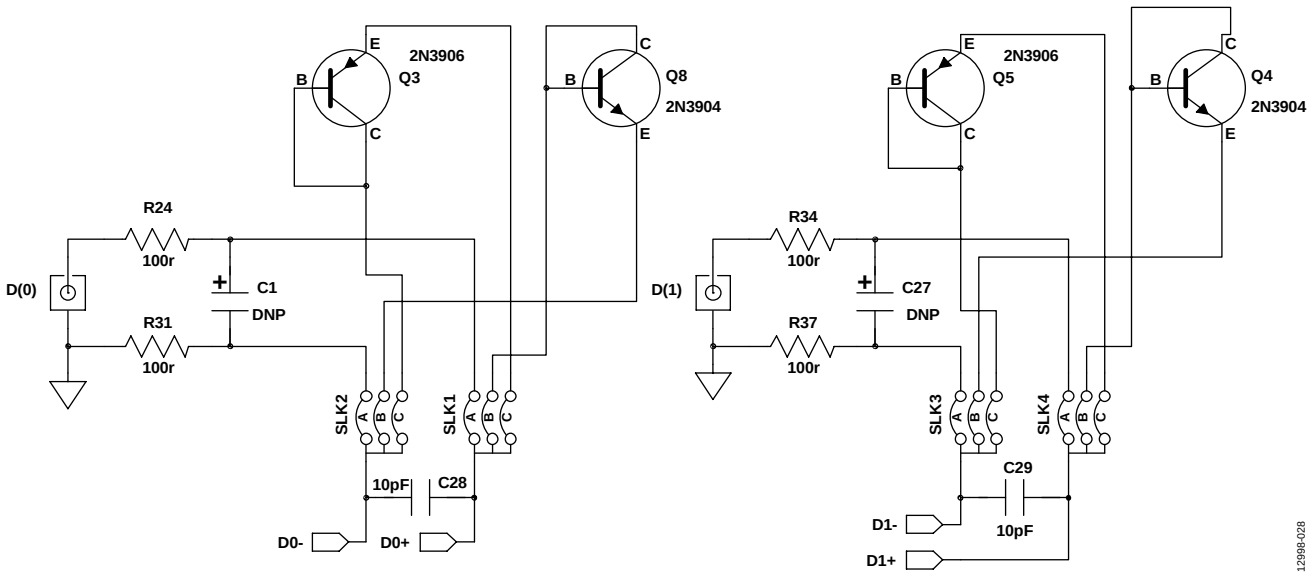


Figure 30. EVAL-AD7293SDZ Schematic, Temperature Sensors Block

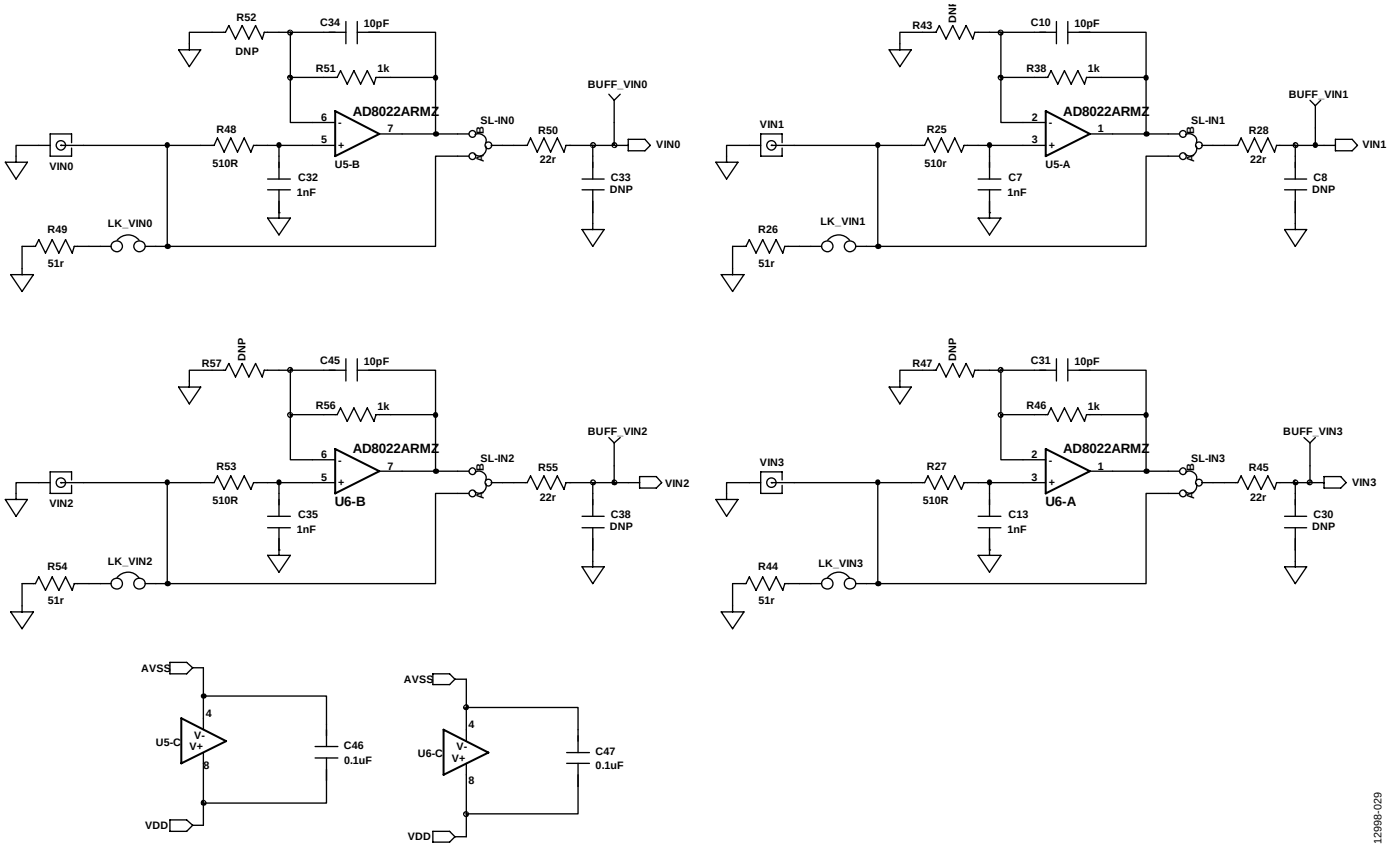


Figure 31. EVAL-AD7293SDZ Schematic, ADC Inputs Block

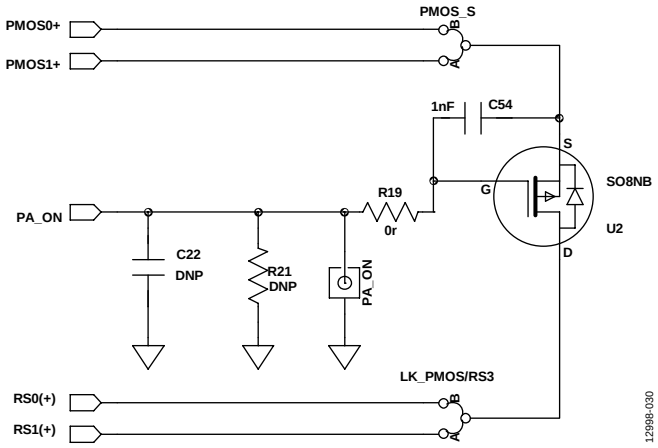


Figure 32. EVAL-AD7293SDZ Schematic, PMOS Switch Controlled by PA_ON Block

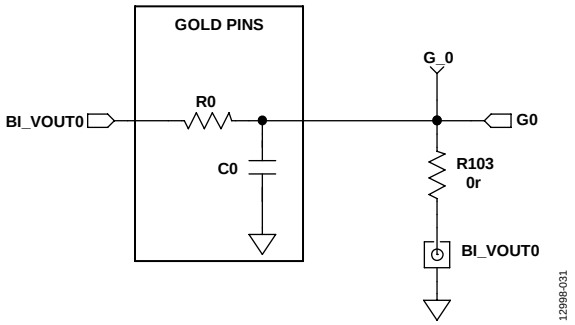


Figure 33. EVAL-AD7293SDZ Schematic, BI_VOUT0 Filter Block

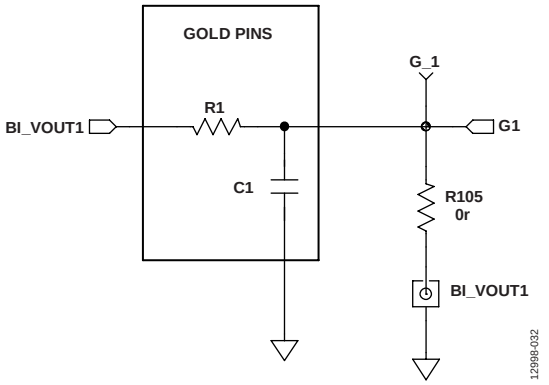


Figure 34. EVAL-AD7293SDZ Schematic, BI_VOUT1 Filter Block

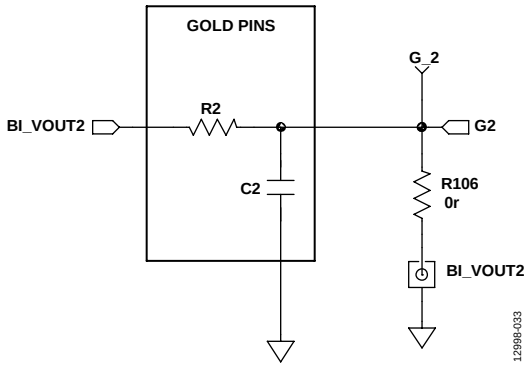


Figure 35. EVAL-AD7293SDZ Schematic, BI_VOUT2 Filter Block

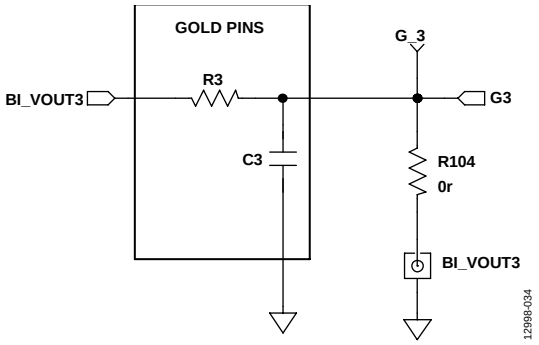


Figure 36. EVAL-AD7293SDZ Schematic, BI_VOUT3 Filter Block

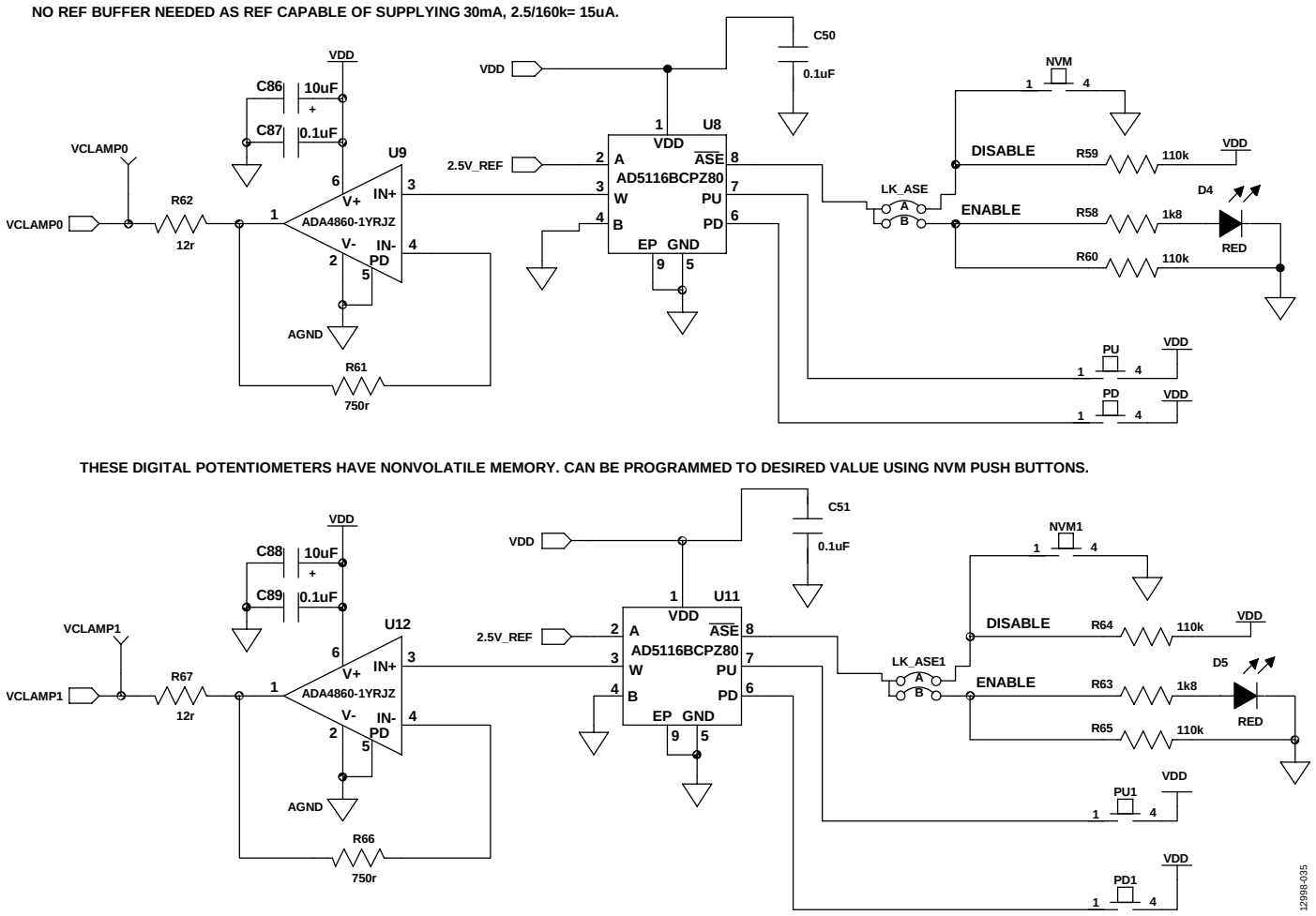
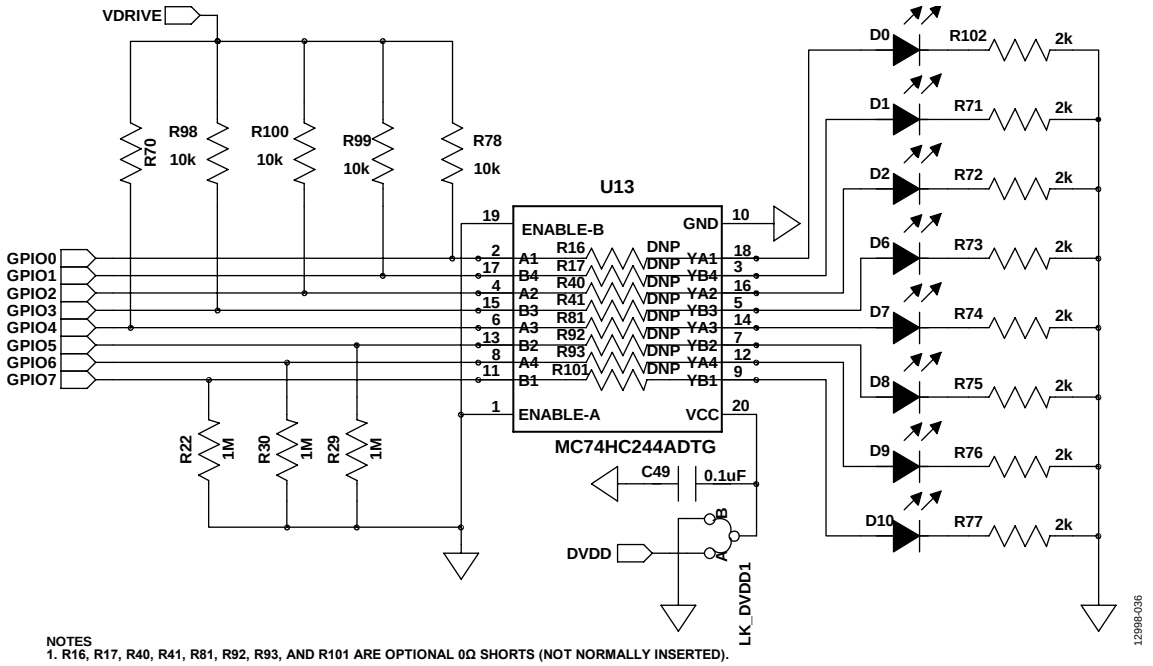


Figure 37. EVAL-AD7293SDZ Schematic, VCLAMP Input Voltage Block



NOTES
1. R16, R17, R40, R41, R81, R92, R93, AND R101 ARE OPTIONAL 0Ω SHORTS (NOT NORMALLY INSERTED).

Figure 38. EVAL-AD7293SDZ Schematic, LED Indicator Block

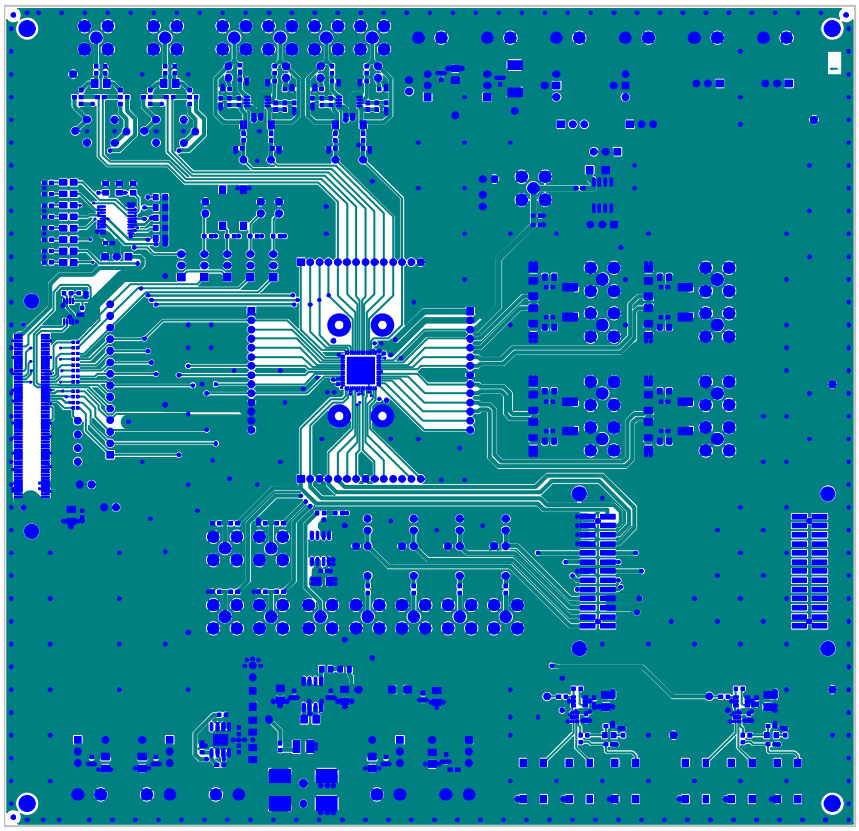


Figure 39. EVAL-AD7293SDZ Evaluation Board Layout, Component Side View

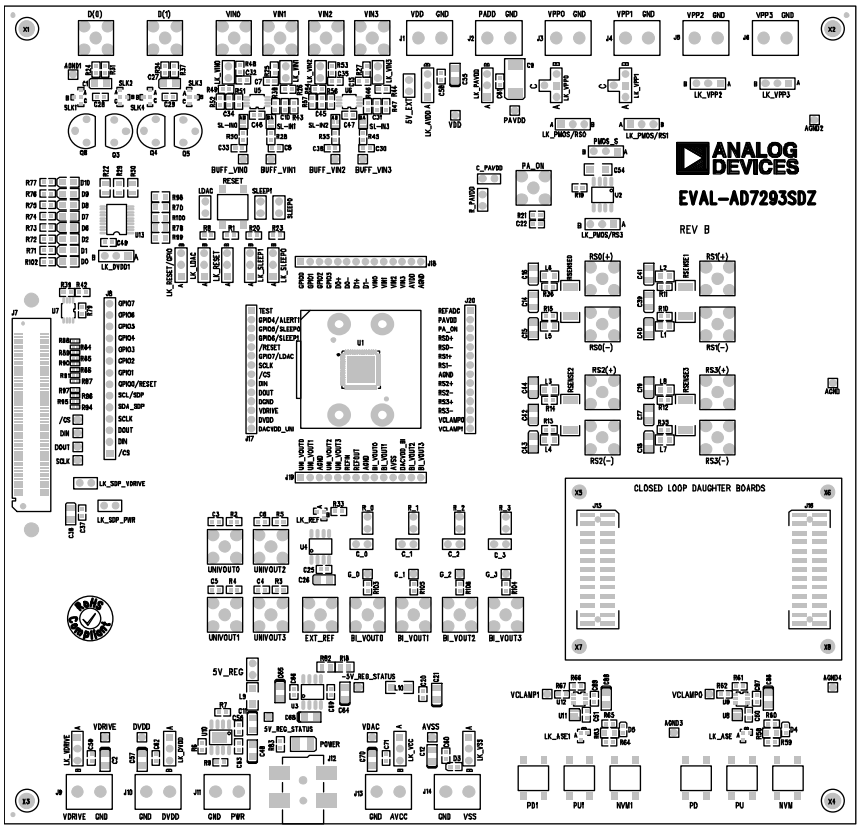


Figure 40. EVAL-AD7293SDZ Evaluation Board Layout, Silkscreen View

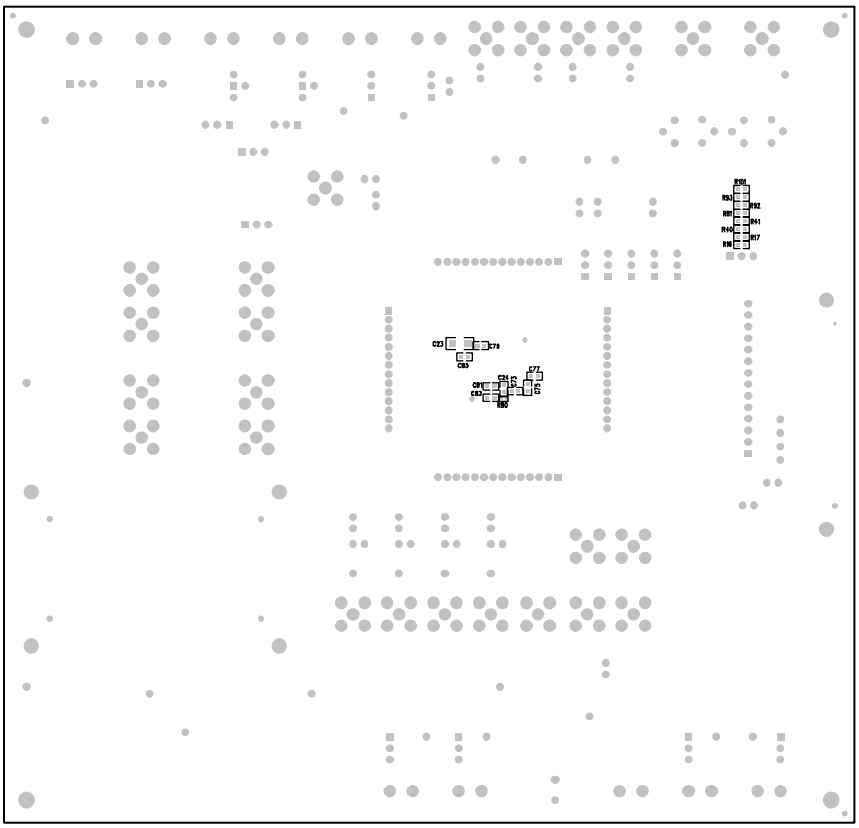


Figure 41. EVAL-AD7293SDZ Evaluation Board Layout, Solder Side View

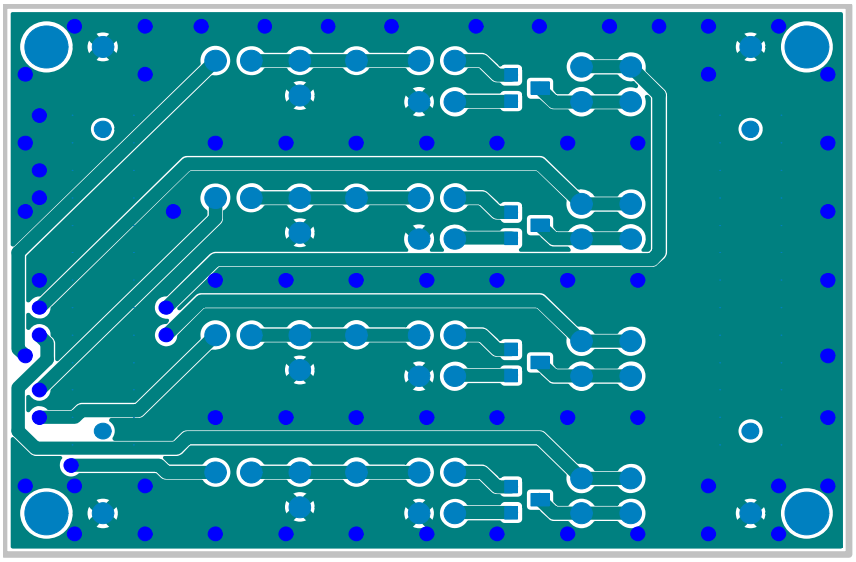


Figure 42. EVAL-AD7293SDZ Daughter Board Layout, Component Side View

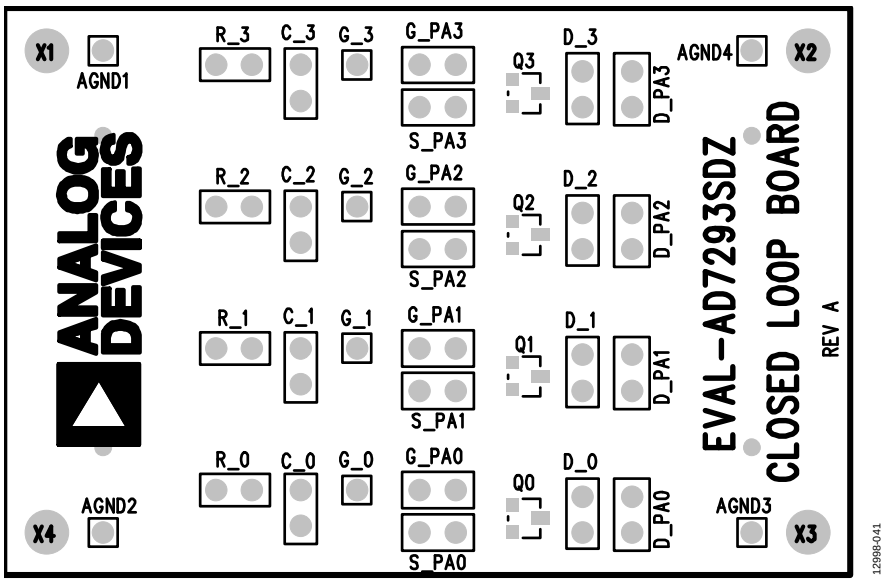


Figure 43. EVAL-AD7293SDZ Daughter Board Layout, Silkscreen View

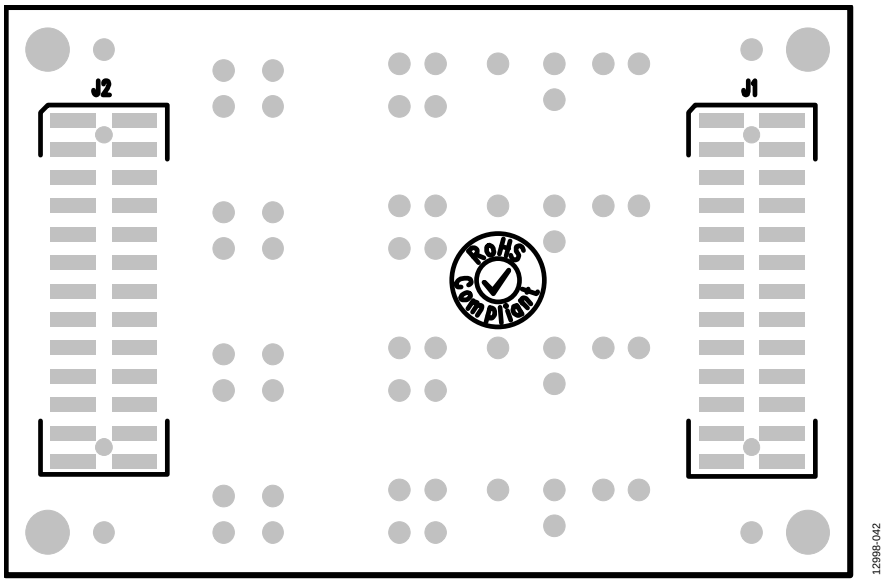


Figure 44. EVAL-AD7293SDZ Daughter Board Layout, Solder Side View

ORDERING INFORMATION

BILL OF MATERIALS

Table 12. Daughter Board Bill of Materials

Reference Designator	Description	Manufacturer	Part Number
AGND1 to AGND4	Red test point	Farnell Electronics, Inc.	8731144
C_0 to C_3, D_0 to D_3, R_0 to R_3	Socket pin, PCB, PK100 (two pins only)	Farnell Electronics	329563
D_PA0 to D_PA3, G_PA0 to G_PA3, S_PA0 to S_PA3	2-pin (0.1 inch pitch) header and shorting shunt	Farnell Electronics	1022247, 150411
G_0 to G_3	Black test point	Farnell Electronics	8731128
J1	Header, 26-pin (2 × 13), 2 mm pitch SMD	Digi-Key	SAM1167-13-ND
J2	Receptacle, 26-pin (2 × 13), 2 mm pitch SMD	Digi-Key	MMS-113-02-L-DV-P-ND
Q0 to Q3	MOSFET, N, depletion mode	Farnell Electronics	1471702

Table 13. Evaluation Board Bill of Materials

Reference Designator	Description	Manufacturer	Part Number
−5V_REG_STATUS, /CS, 5V_REG_STATUS, AGND, AGND1 to AGND4, BUFF_VIN0 to BUFF_VIN3, DIN, DOUT, SCLK	Red test points	Farnell Electronics	8731144
5V_EXT, 5V_REG, LDAC, LK_SDP_PWR, LK_SDP_VDRIVE, LK_VIN0 to LK_VIN3	2-pin (0.1 inch pitch) headers and shorting shunts	Farnell Electronics	1022247, 150411
AVSS, DVDD, G_0 to G_3, PAVDD, VCLAMP0 to VCLAMP1, VDAC, VDD, VDRIVE	Black test points	Farnell Electronics	8731128
BI_VOUT0 to BI_VOUT3, PA_ON, RS0(+)/RS0(−) to RS3(+)/RS3(−), UNIVOUT0 to UNIVOUT3	50 W, gold plated PCB, SMA jacks	Farnell Electronics	1248990
C1, C3 to C6, C8, C14 to C19, C22, C27, C30, C33, C38 to C44, L1 to L8, R16, R17, R21, R33, R39 to R41, R43, R47, R52, R57, R81, R92, R93, R101	Do not insert	Do not insert	
C2, C11, C12, C21, C26, C36, C48, C55, C57, C64, C65, C68, C70, C86, C88	Capacitors, Case A, 10 µF, 10 V	Farnell Electronics	197130
C7, C13 ,C32, C35	50 V, X7R, multilayer ceramic capacitors	Farnell Electronics	9406174
C9	Capacitors, Case D, 10 µF, 50 V	Farnell Electronics	2250169
C10, C28, C29, C31, C34, C45	50 V, NPO, multilayer ceramic capacitors	Farnell Electronics	499110
C23	Capacitors, MLCC, X7R, 4.7 µF, 50 V, 1206	Farnell Electronics	1908177
C20, C24, C25, C37, C46, C47, C49 to C51, C58 to C60, C56, C62, C63, C66, C69, C71, C73, C75, C77, C79, C81, C83, C87, C89	Capacitors, 0603, 0.1 µF, 16 V, X7R	Farnell Electronics	9406140
C54	50 V, X7R, multilayer ceramic capacitors	Farnell Electronics	1759337
C61, C85	Capacitors, 0603, 0.1 µF, 100 V, X7R	Farnell Electronics	1828921
C_0 to C_3, C_PAVDD, R_0 to R_3, R_PAVDD	Socket pins, PCB, PK100 (two pins only)	Farnell Electronics	329563
D0x, D1x, VIN0 to VIN3	50 W, gold plated PCB, SMB jacks	Farnell Electronics	1206013
D0 to D2, D6 to D10, POWER	Red SMD LEDs	Farnell Electronics	5790840
D3	Diode, Schottky, 30 V, 200 mA, 0603	Farnell Electronics	2211954
D4, D5	Red SMD LEDs	Farnell Electronics	1685068
EXT_REF	50 W, gold plated PCB, SMB jacks	Do not insert	Do not insert
J1 to J6, J9 to J11, J13, J14	2-pin terminal blocks (5 mm pitch)	Farnell Electronics	151789
J7	120-way connector, 0.6 mm pitch	Farnell Electronics	1324660
J8	Connector, header, THT, 2.54 mm, 36-way (cut to 14-pin)	Farnell Electronics	1022264
J12	DC power connectors, 2 mm SMT power jack	Mouser Electronics	806-KLDX-SMT20202A
J15	Receptacle, 26-pin, (2 × 13) 2 mm pitch SMD	Digi-Key	MMS-113-02-L-DV-P-ND
J16	Header, 26-pin, (2 × 13), 2 mm pitch SMD	Digi-Key	SAM1167-13-ND
J17 to J20	14-pin SIL headers, 2 mm pitch	Digi-Key	M22-2011405-ND
L9, L10	Inductor, SMD, 600Z	Farnell Electronics	9526862

Reference Designator	Description	Manufacturer	Part Number
LK_ASE, LK_ASE1, LK_REF	2-way solder links (use 0 Ω, 0603 resistors)	Farnell Electronics	9331662
LK_AVDD, LK_DVDD, LK_DVDD1, LK_LDAC, LK_PAVDD, LK_PMOS/RS0, LK_PMOS/RS1, LK_PMOS/RS3, LK_RESET, LK_RESET/GPIO, LK_SLEEP0, LK_SLEEP1, LK_VCC, LK_VDRIVE, LK_VPP2, LK_VPP3, LK_VSS, PMOS_S	3-pin SIL headers and shorting links	Farnell Electronics	1022248, 150410
LK_VPP0, LK_VPP1	4-pin (3 + 1) headers (cut to size) and shorting links	Farnell Electronics	1022264, 150410
NVM, NVM1, PD, PD1, PU, PU1, RESET	SMD push button switches (sealed 6 mm × 6 mm)	Farnell Electronics	177807
Q3, Q5	Transistors, 45 V, 200 mA, PNP, TO-92	Farnell Electronics	1574372
Q4, Q8	Transistors, NPN, 40 V, 200 mA, TO-92	Farnell Electronics	9846743
R1, R8, R20, R23	Resistors, 10 kΩ, 0.063 W, 1%, 0603	Farnell Electronics	9330399
R2 to R5, R9, R10 to R15, R19, R35, R36, R103 to R106, SL-IN0 to SL-IN3, SLK1 to SLK4	Resistors, 0603, 1%, 0 Ω	Farnell Electronics	9331662
R6, R7, R42, R79	Resistors, 100 kΩ, 0.063 W, 1%, 0603	Farnell Electronics	9330402
R18	Resistor, 1.6 kΩ, 0.1 W, 1%, 0805	Farnell Electronics	9332669
R22, R29, R30	Resistors, 1 MΩ, 0.1 W, 1%, 0805	Farnell Electronics	9332413
R24, R31, R34, R37	Resistors, 100 Ω, 0.063 W, 1%, 0603	Farnell Electronics	9330364
R25, R27, R48, R53	Resistors, 510 Ω, 0.063 W, 1%, 0603	Farnell Electronics	9331298
R26, R44, R49, R54	Resistors, 51 Ω, 0.063 W, 1%, 0603	Farnell Electronics	9331336
R28 R45, R50, R55	Resistors, 22 Ω, 0.063 W, 1%, 0603	Farnell Electronics	9330844
R38, R46, R51, R56	Resistors, 1 kΩ, 0.063 W, 1%, 0603	Farnell Electronics	9330380
R58, R63	Resistors, 1.8 kΩ, 0.1 W, 1%, 0805	Farnell Electronics	9332715
R59, R60, R64, R65	Resistors, 110 kΩ, 0.063 W, 1%, 0603	Farnell Electronics	9330461
R61, R66	Resistors, 750 Ω, 0.063 W, 1%, 0603	Farnell Electronics	9331506
R62, R67	Resistors, 12 Ω, 0.063 W, 1%, 0603	Farnell Electronics	9330534
R70, R78, R98 to R100	Resistors, 10 kΩ, 0.1 W, 1%, 0805	Farnell Electronics	9332391
R71 to R77, R83, R102	Resistors, 2 kΩ, 0.063 W, 1%, 0603	Farnell Electronics	9330763
R80, R84 to R91, R94 to R97	Resistors, 0402, 1%, 0 Ω	Farnell Electronics	1357983
R82	Resistor, 30 kΩ, 0.1 W, 1%, 0805	Farnell Electronics	9333002
RSENSE0 to RSENSE3	Resistors thin film, 100 Ω, 0.1%, 2512	Farnell Electronics	2325372
SLEEP0, SLEEP1	2-pin (0.1-inch pitch) headers and shorting shunts	Farnell Electronics	1022247, FEC 150411
U1	AD7293BCPZ	Analog Devices, Inc.	AD7293BCPZ
U2	MOSFET P-CH, 30 V, 8.1 A, SOIC8	Farnell Electronics	1858951
U3	120 mA switched capacitor voltage inverter with regulated output	Analog Devices	ADP3605ARZ-R7
U4	Ultralow noise XFET voltage reference	Analog Devices	ADR431BRZ
U5, U6	Dual op amps	Analog Devices	AD8022ARMZ
U7	32 kb, I²C serial EEPROM	Farnell Electronics	1331330
U8, U11	Digital potentiometers, 64 taps, 8% resistor tolerance	Analog Devices	AD5116BCPZ80-500R7
U9, U12	Precision rail-to-rail op amps	Analog Devices	ADA4860-1YRJZ
U10	Linear regulator 5 V, 20 V, 500 mA, ultralow noise, CMOS	Analog Devices	ADP7104ARDZ-5.0-R7
U13	74 HC CMOS, SMD, 74HC244, TSSOP20	Farnell Electronics	1104721

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

www.analog.com